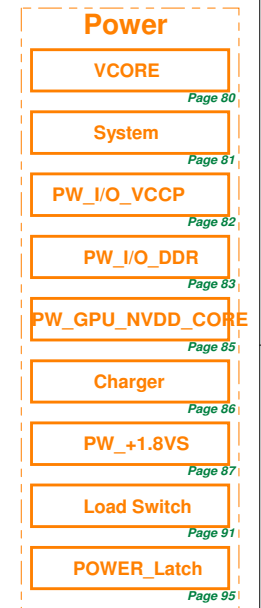
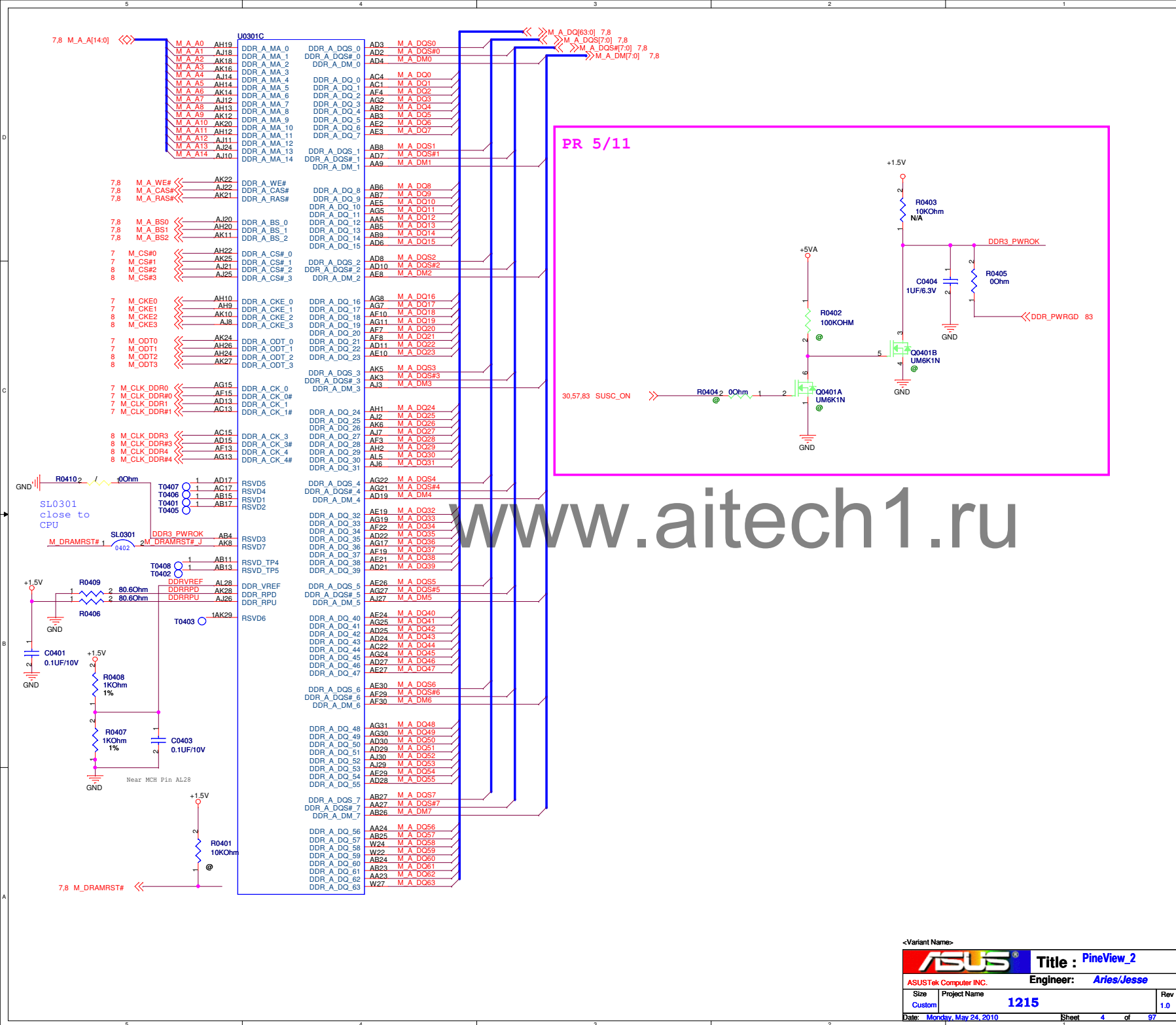


1215 SCHEMATIC Revision 1.1

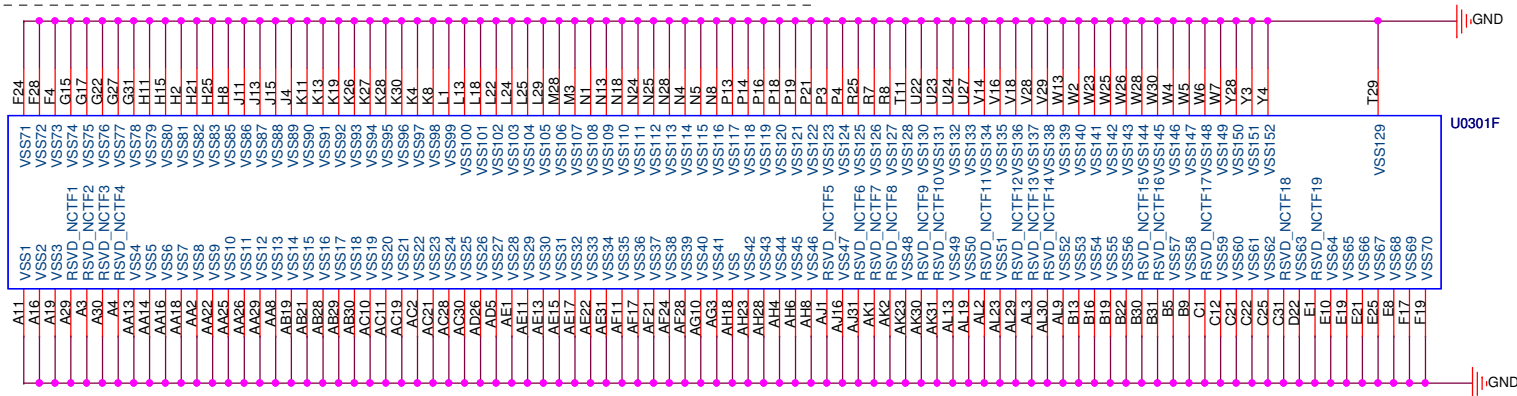
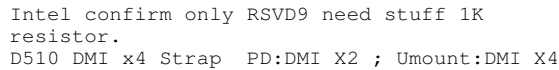
[illegible]

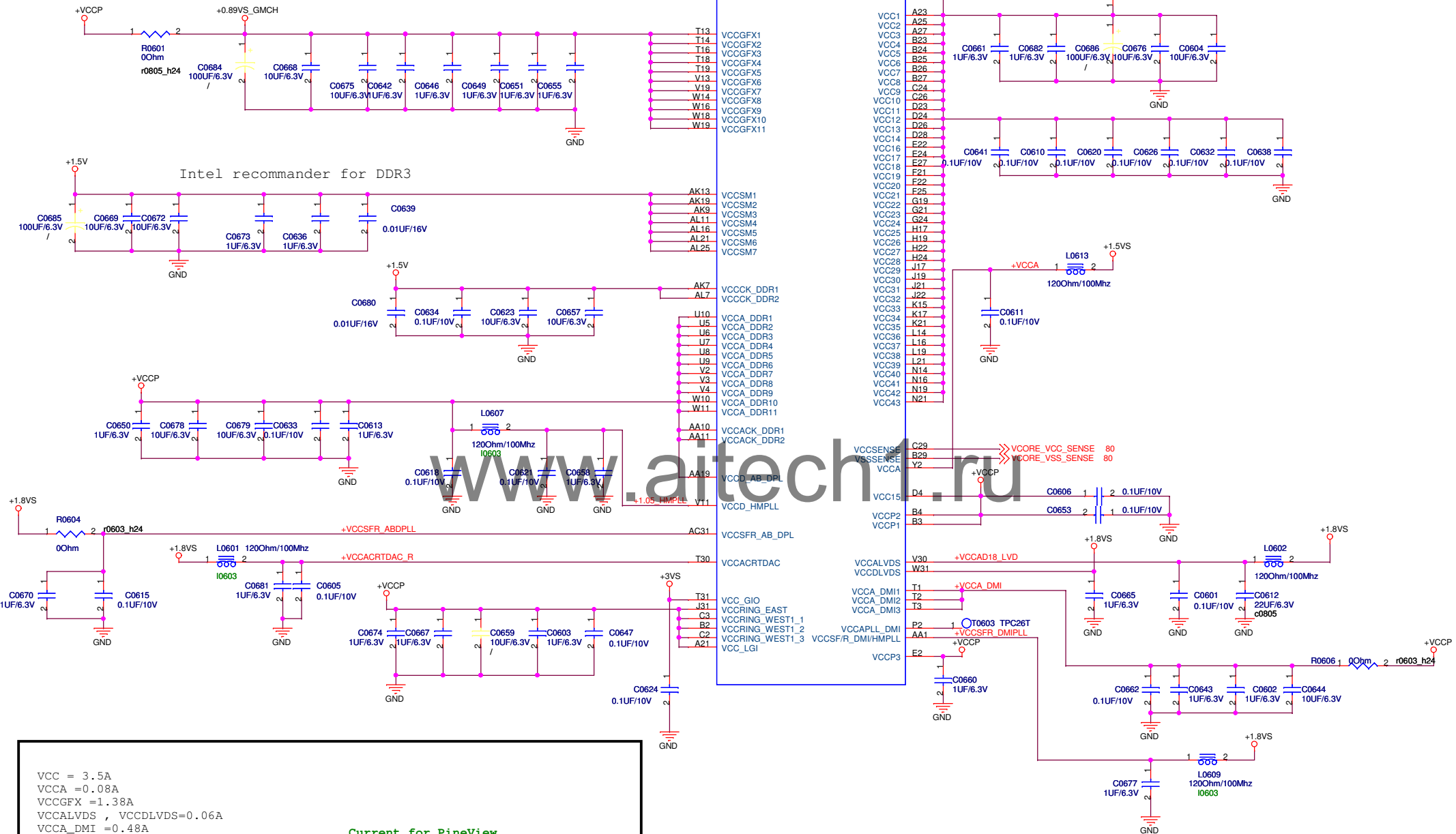
BLOCK DIAGRAM





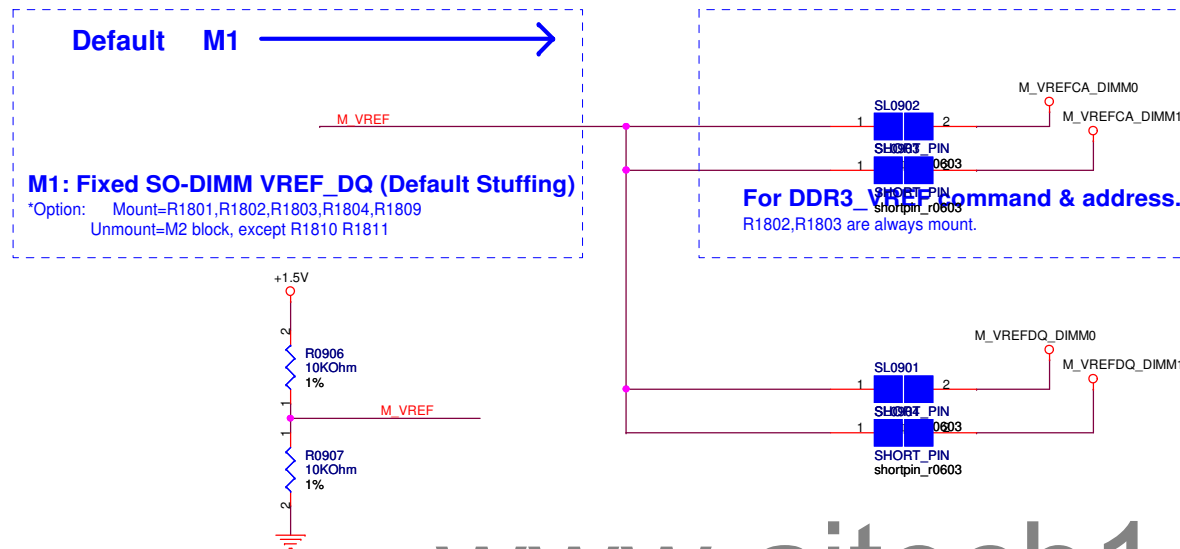
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VCC = 3.5A
 VCCA = 0.08A
 VCCGFX = 1.38A
 VCCALVDS, VCCDLVDS = 0.06A
 VCCA_DMI = 0.48A
 VCCSFR_DMIHPLL = 0.104A
 VCCA_DDR and VCCACK_DDR = 1.32A
 VCCSM and VCCCK_DDR = 2.27A
 VCCRING_EAST, VCCRING_EAST_WEST, VCC_LGI, VCCD_AB_DPL, VCCD_HMPLL = 0.33A
 VCC_GIO = 0.006A
 VCCSFR_AB_DPL, VCCACRTDAC = 0.154A

Current for PineView




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		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: ***	
Size	Project Name		Rev
A	1215		1.00
Date: Monday, May 24, 2010		Sheet	14 of 97

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		Title :	
ASUSTeK COMPUTER INC. NB6		Engineer: ***	
Size A	Project Name 1215		Rev 1.00
Date: Monday, May 24, 2010		Sheet	15 of 97

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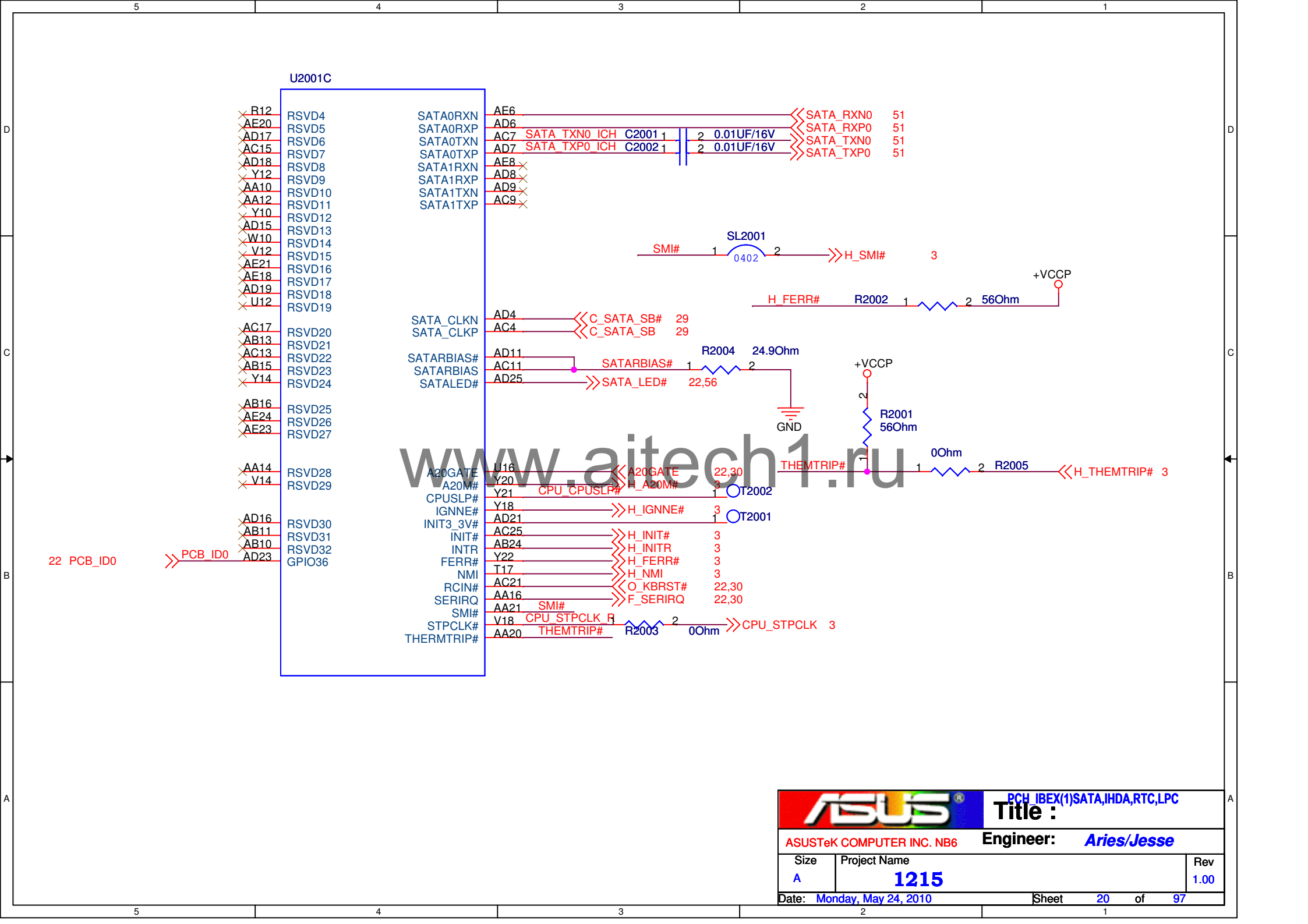
<Variant Name>		
		Title : DDR2-SO-DIMM
ASUSTek Computer INC.		Engineer: ***
Size C	Project Name 1215	Rev 1.2G
Date: Monday, May 24, 2010		Sheet 16 of 87

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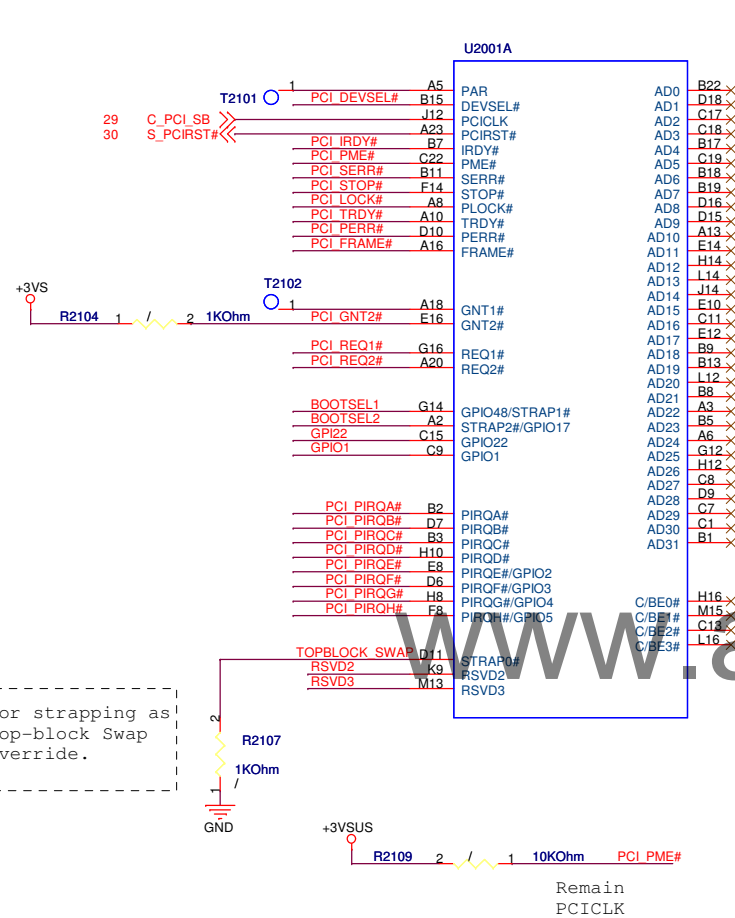
www.aitech1.ru

		Title DDR3 Vref	
ASUSTeK COMPUTER INC. NB6		Engineer: ***	
Size C	Project Name 1215		Rev 1.00
Date: Monday, May 24, 2010 Sheet 18 of 97			

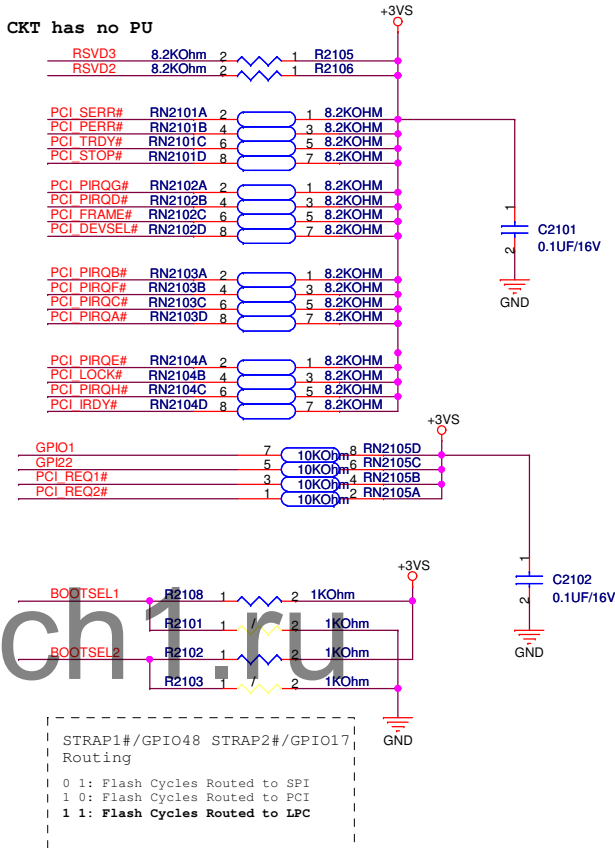
www.aitech1.ru



For strapping as
Top-block Swap
override.



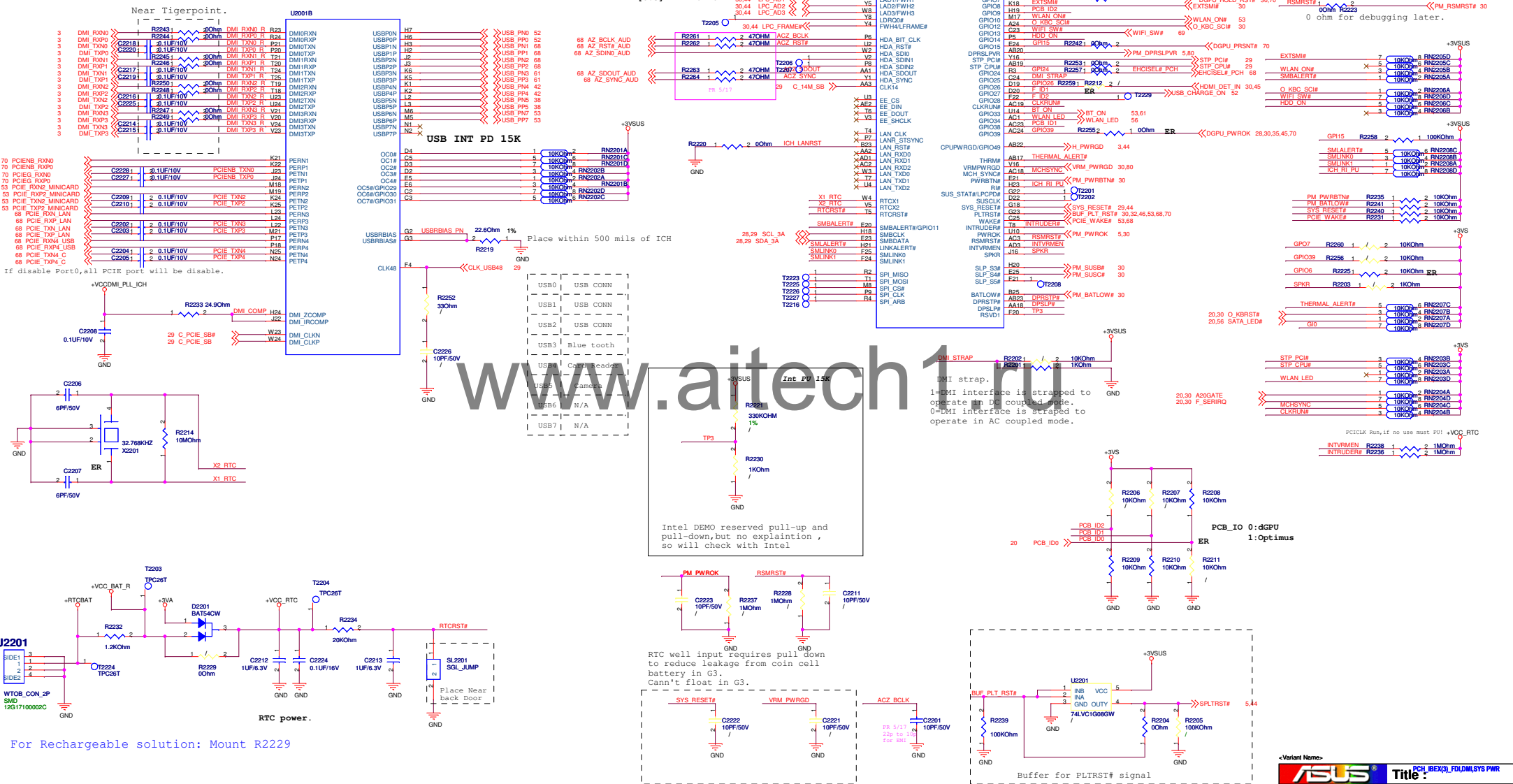
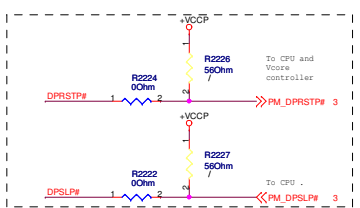
In P-D Demo KKT has no PU




<Variant Name>

ASUS		PCH (BEX(2) PCIE,CLK,SM6,PEG)	
ASUSTek Computer INC.		Title: Aries/Jesse	
Size B	Project Name 1215	Rev 1.0	
Date: Monday, May 24, 2010		Sheet 21 of 97	

SATA RX,TX all need AC couple and place near Connector side for signal quality.And Traces to them should match length. ICH7M need pull down RX, if no use.




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		Title	
ASUSTeK COMPUTER INC. N96		H1819(4) DP, LVDS, CRT	
Engineer: ***			
Size	Project Name		Rev
C	1215		1.00
Date: Monday, May 24, 2010		Sheet	23 of 97

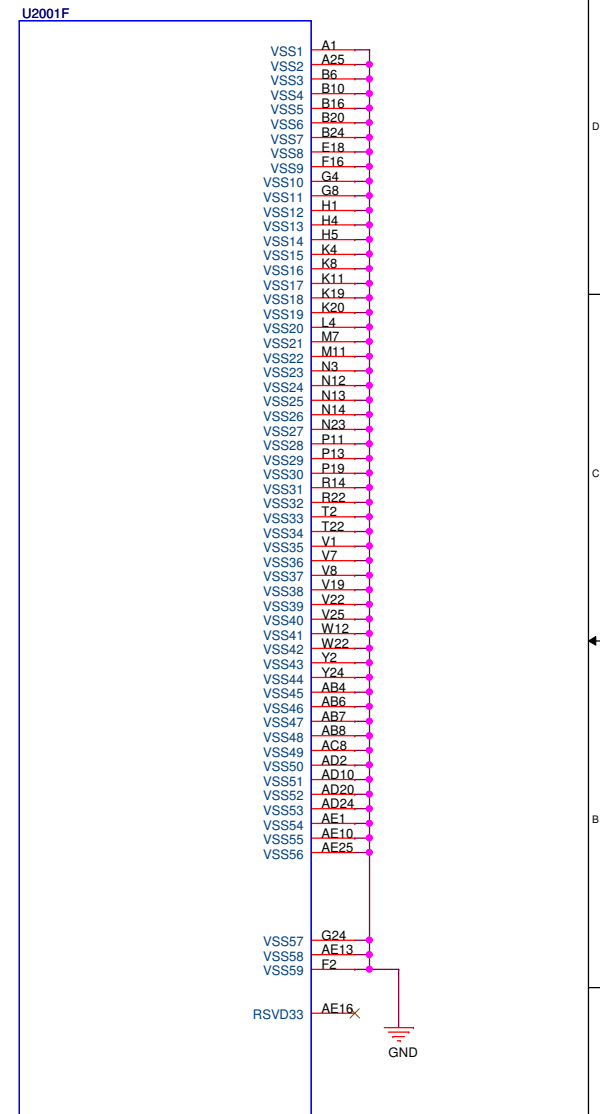
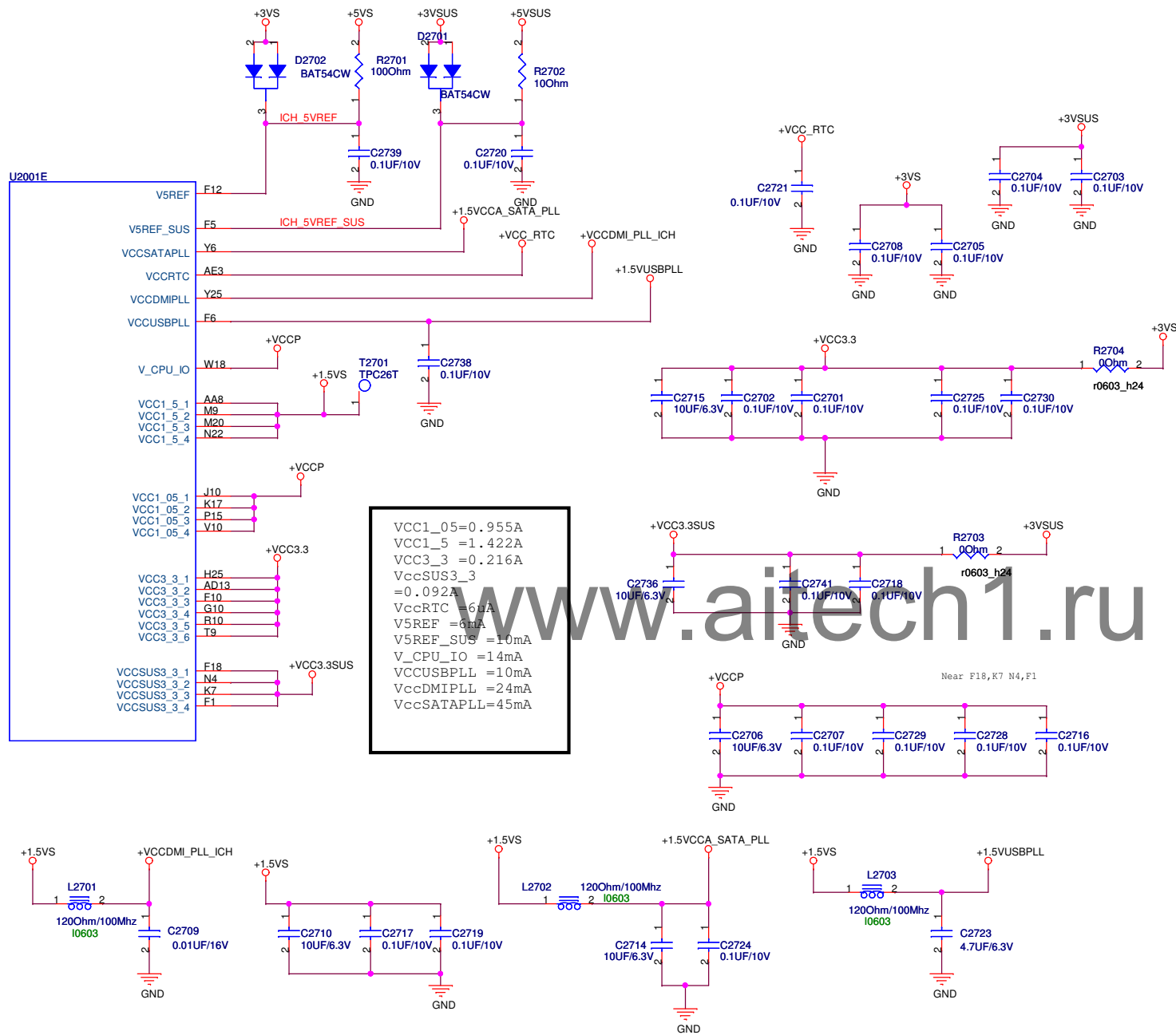
www.aitech1.ru

		CHVRAM.USB	
ASUSTeK COMPUTER INC. N86		Engineer: ***	
Size C	Project Name 1215		Rev 1.00
Date: Monday, May 24, 2010		Sheet	24 of 97

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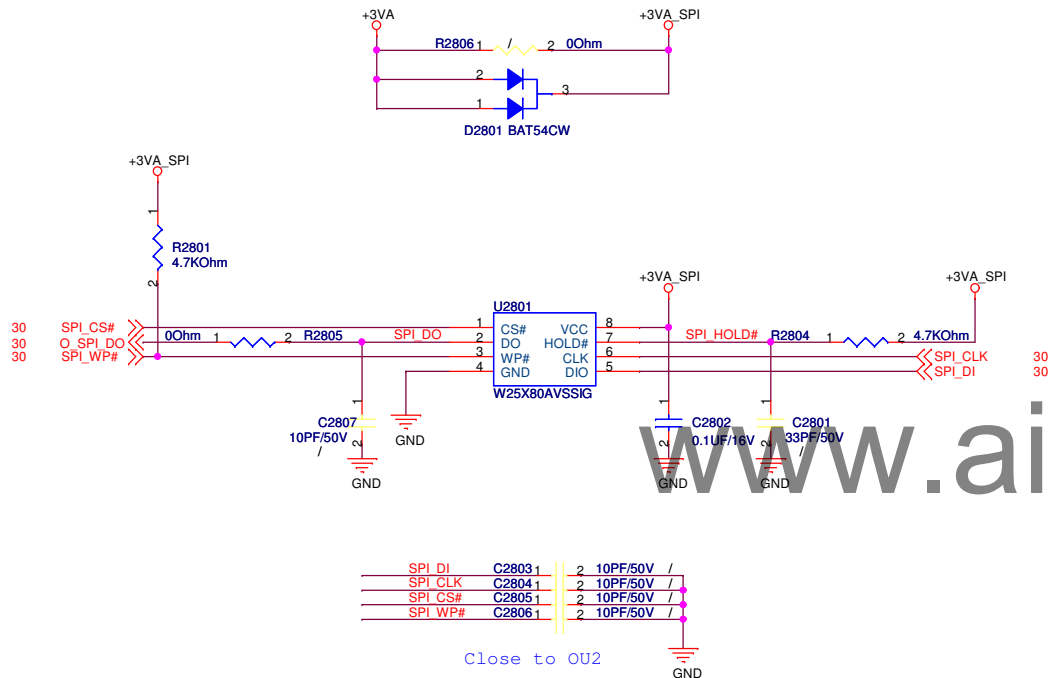
		Title : PCH_IBEX(6)CPU_GPIO,MISC,GND	
ASUSTeK COMPUTER INC. N66		Engineer: CH_Lin	
Size C	Project Name UL30AD		Rev 1.00
Date: Monday, May 24, 2010		Sheet 25 of 97	

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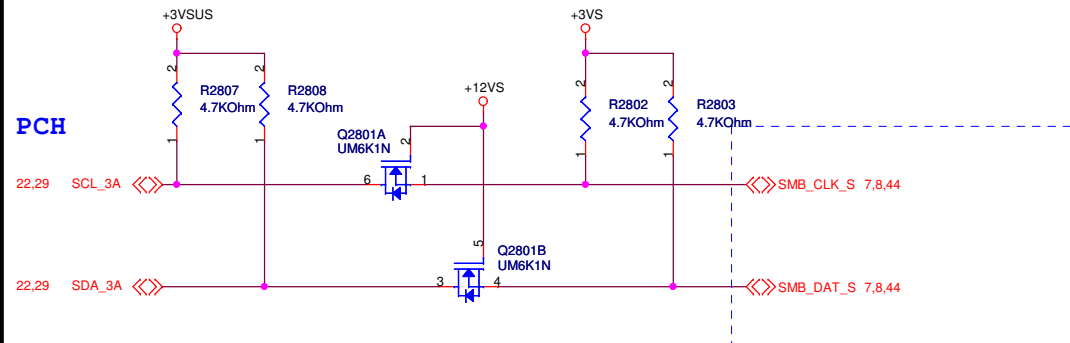
PCH SPI ROM

No SPI FLASH TOOL CON



SMBUS Link device:

SPD, CLKGEN, CPU XDP, PCH XDP, VID CONTROLLER, DDRVref



EC, G780

ASUS		Title :PCH_SPI ROM,OTH	
ASUSTeK COMPUTER INC. NB6		Engineer: Aries/Jesse	
Size Custom	Project Name 1215		Rev 1.00
Date: Monday, May 24, 2010		Sheet 28 of 97	

1:Disable
0:Enable

PEREQ1:PCIEx0 &
PCIEx1
PEREQ2:PCIEx2 &
PCIEx3 & SATA
PEREQ3:PCIEx4 &
PCIEx5 & PCIeX6

FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

C LAN 25M	PR 5/17	C2928 2	1	33PF/50V
C SATA_SB		C2916 2	1	10PF/50V
C SATA_SB#		C2917 2	1	10PF/50V
CLK_PCIE_USB_PCH		C2918 2	1	10PF/50V
CLK_PCIE_USB#_PCH		C2919 2	1	10PF/50V
C_LCD_LVDS#		C2920 2	1	10PF/50V
C_LCD_LVDS		C2921 2	1	10PF/50V
STP_PCIF#		C2934 2	1	10PF/50V
STP_CPU#		C2930 2	1	10PF/50V
C_PCI_SB_R		C2909 2	1	10PF/50V
FS4		C2910 2	1	10PF/50V
SDA_3A		C2931 2	1	10PF/50V
SCL_3A		C2932 2	1	10PF/50V
C_DOC_REQ		C2933 2	1	10PF/50V
C_FSLC		C2911 2	1	10PF/50V
C_FSLA	ER	C2913 2	1	33PF/50V
C_48M_R	ER	C2908 2	1	33PF/50V
C LAN 25M_R		C2927 2	1	10PF/50V

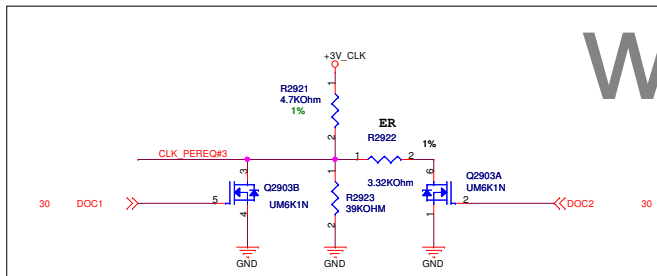
For RF,EMI

C FSLB	R2929 1	2	10KOhm
STP_CPU#	R2950 1	2	10KOhm
C_FSLC	R2919 2	1	8.2KOhm
C_48M_R	R2920 2	1	8.2KOhm

C_FSLA	R2934	2	1	8.2KOhm/200M

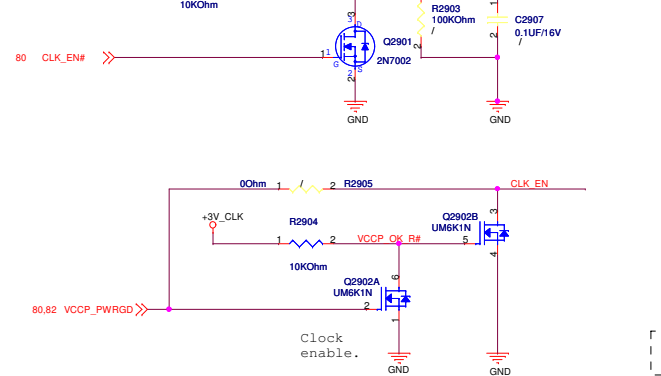
FS4	R2906 2	1	8.2KOhm
	R2931 2	1	8.2KOhm

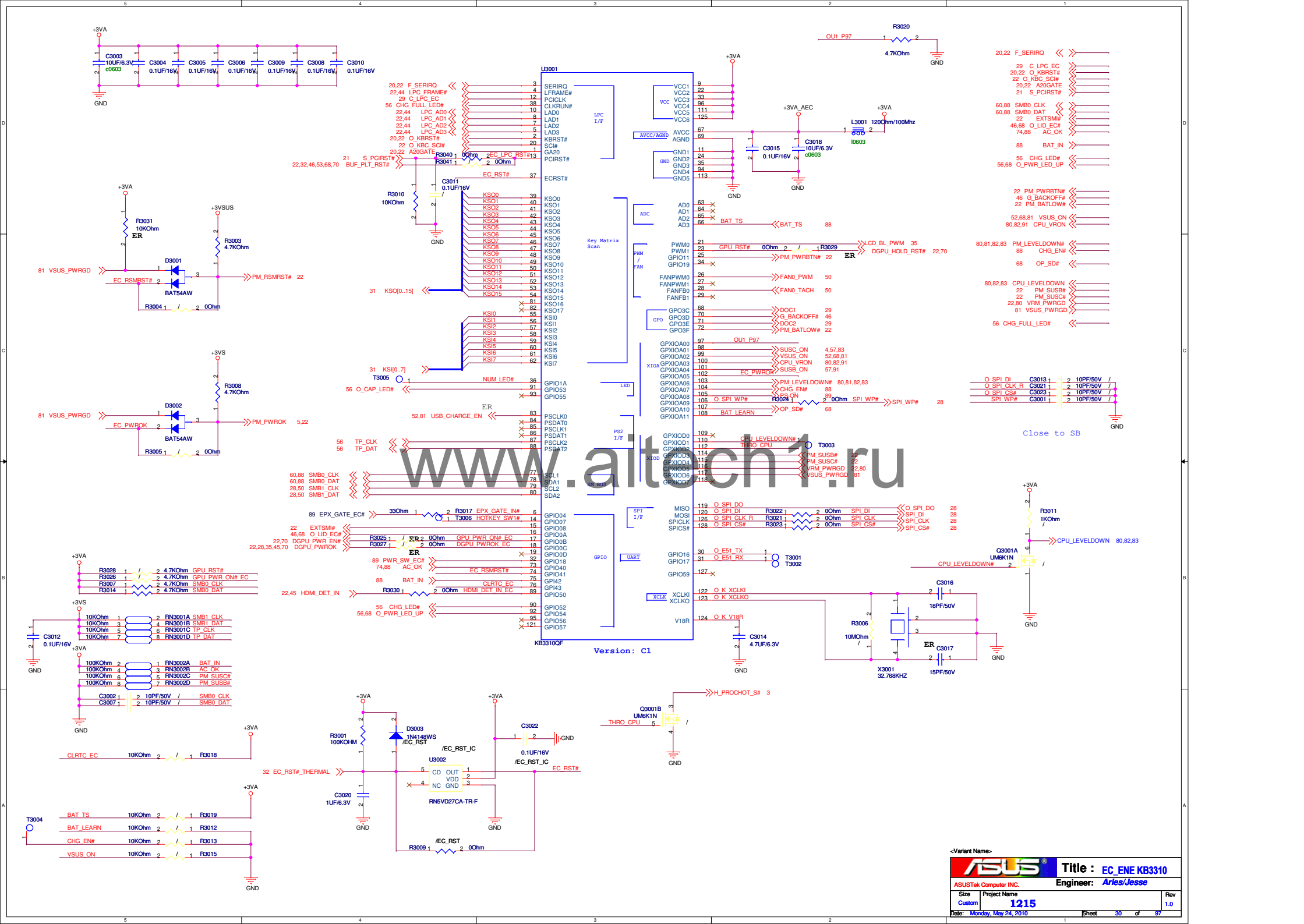
FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133
0	1	0	200



O_DOC1	O_DOC2	Voltage	Status
L	L	2.4-3.3V	Super
L	H	0.5-2.36V	Normal
H	*	0-0.35V	Power saving

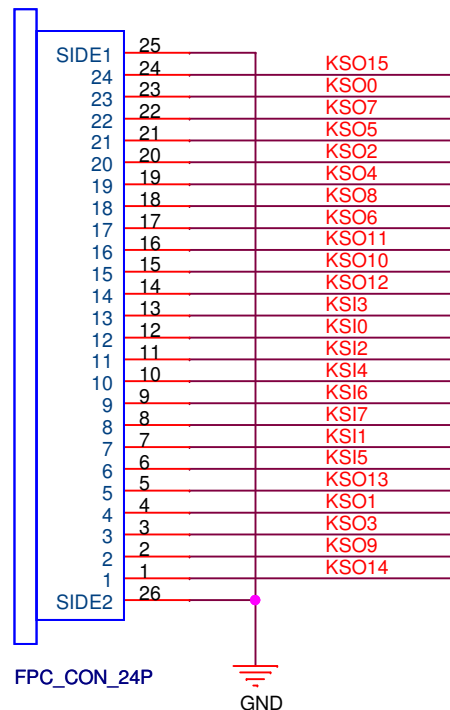
www.aitech1.ru



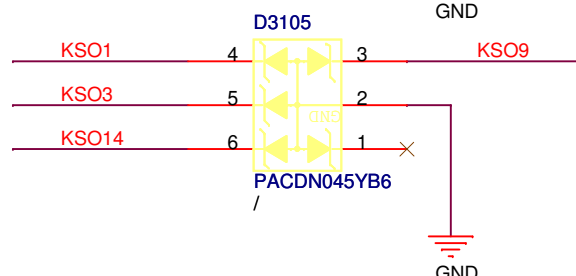
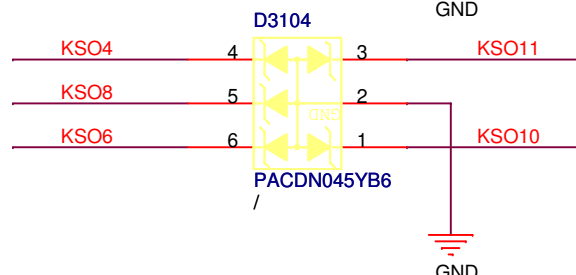
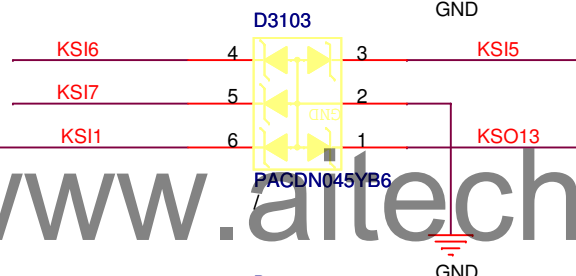
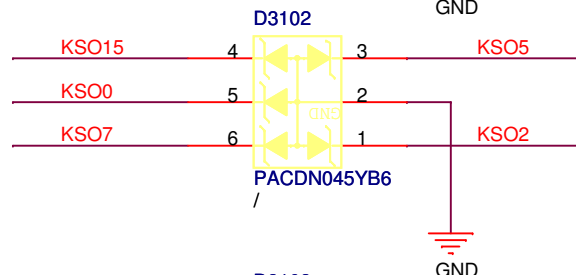
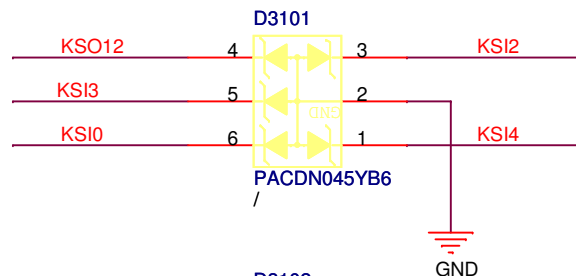


For Keyboard Connector

J3101



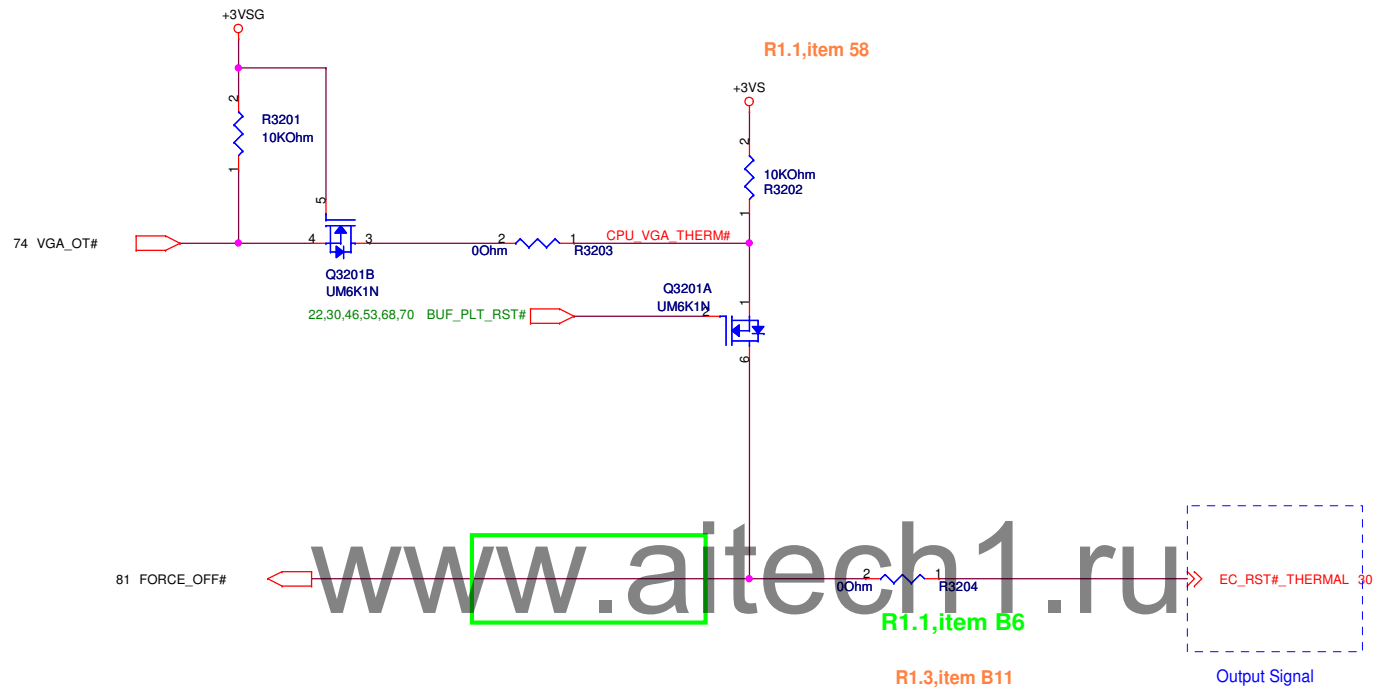
30 KSO[0..15]
30 KSI[0..7]

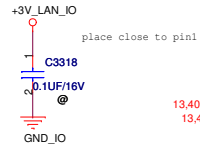
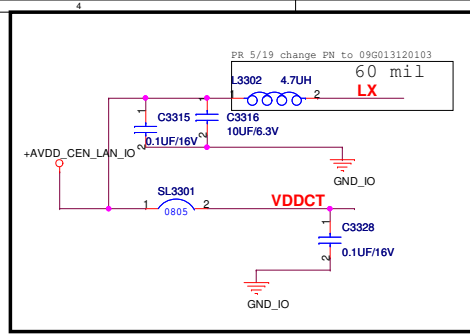


<Variant Name>

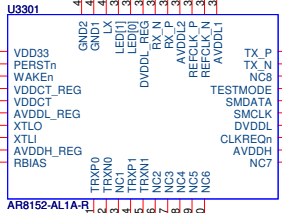
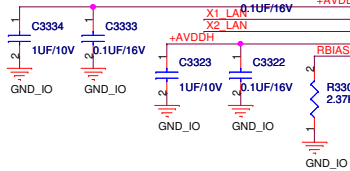
		Title :	KB
ASUSTeK COMPUTER INC		Engineer:	Aries/Jesse
Size	Project Name		Rev
A	1215		1.0
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Thermal Policy

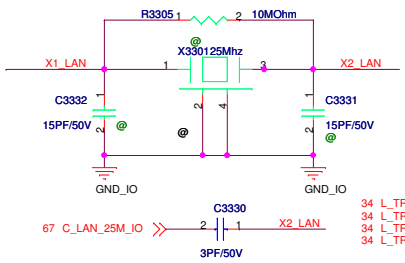
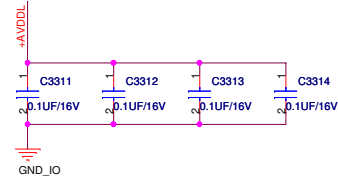
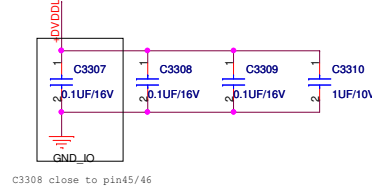
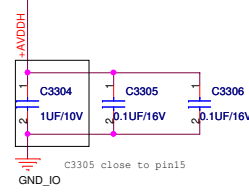
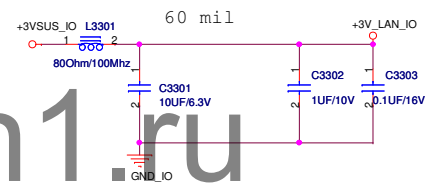
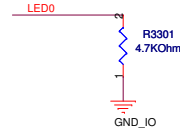




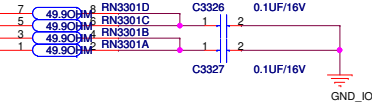
13,40,67 BUF_PLT_RST#_IO
13,40,67 PCIE_WAKE#_IO



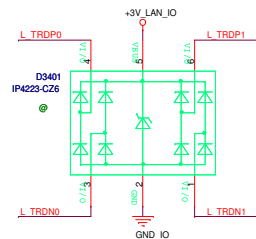
PCIE_TXN_LAN_IO 67
PCIE_TXP_LAN_IO 67
CLK_PCIE_LAN_IO 67
CLK_PCIE_LAN#_IO 67



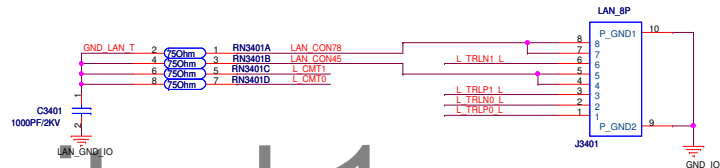
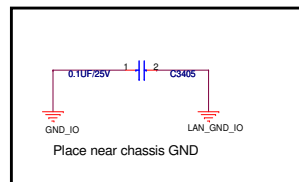
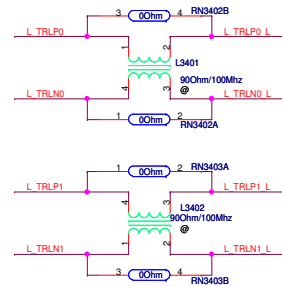
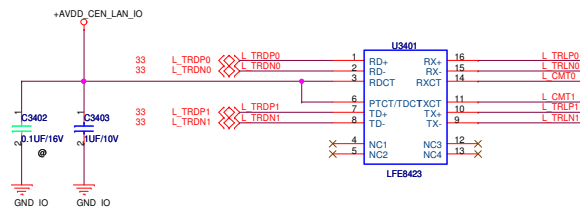
34 L_TRDP0
34 L_TRDN0
34 L_TRDP1
34 L_TRDN1



ASUS		Title :PWR_BUTTON_LED	
ASUSTEK COMPUTER INC		Engineer: Anndy_wang	
Size	Project Name	1005P_IO	Rev
Custom			1.3
Date: Monday, May 24, 2010		Sheet 33 of 97	



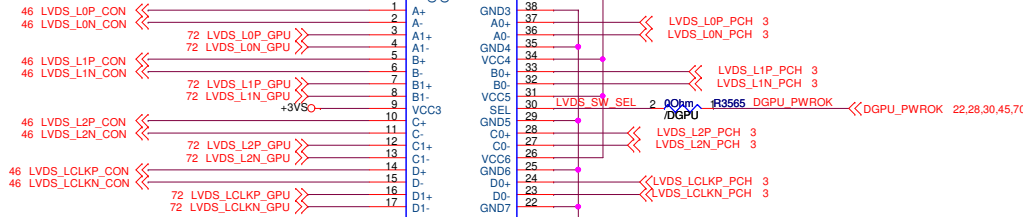
GND_LAN_T 上禁止加任何零件



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LVDS Switch

LVDS_L0P_PCH	/Optimus 1	00hm	2 RN3501A	LVDS_L0P_CON
LVDS_L0N_PCH	/Optimus 3	00hm	4 RN3501B	LVDS_L0N_CON
LVDS_L1P_PCH	/Optimus 1	00hm	2 RN3502A	LVDS_L1P_CON
LVDS_L1N_PCH	/Optimus 3	00hm	4 RN3502B	LVDS_L1N_CON
LVDS_L2P_PCH	/Optimus 1	00hm	2 RN3503A	LVDS_L2P_CON
LVDS_L2N_PCH	/Optimus 3	00hm	4 RN3503B	LVDS_L2N_CON
LVDS_LCLKP_PCH	/Optimus 1	00hm	2 RN3504A	LVDS_LCLKP_CON
LVDS_LCLKN_PCH	/Optimus 3	00hm	4 RN3504B	LVDS_LCLKN_CON

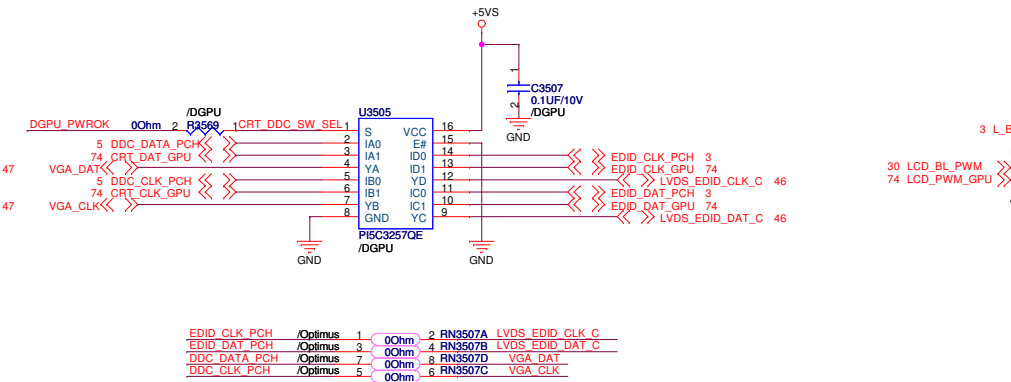


SEL=0 for A0 output (IGPU)
SEL=1 for A1 output (DGPU)

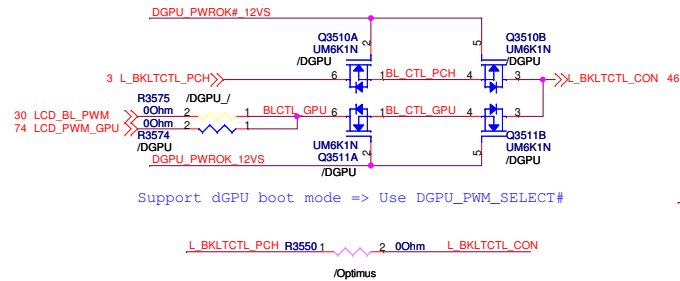
IN=0 for S1 output (IGPU)
IN=1 for S2 output (DGPU)



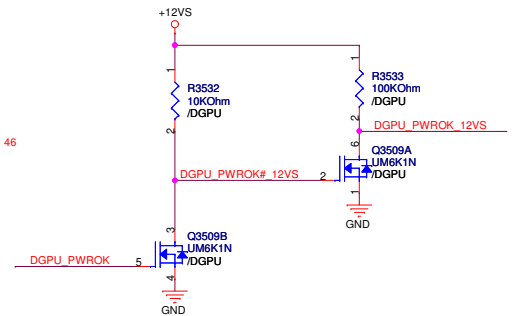
CRT_HSING_PCH	/Optimus 1	00hm	2 RN3508A	CRT_HSING
CRT_VSYNC_PCH	/Optimus 3	00hm	4 RN3508B	CRT_VSYNC
LCD_BACKEN_PCH	/Optimus 1	00hm	2 RN3509A	LCD_BACKEN_CON
L_VDDEN_PCH	/Optimus 3	00hm	4 RN3509B	L_VDDEN_CON



EDID_CLK_PCH	/Optimus 1	00hm	2 RN3507A	LVDS_EDID_CLK_C
EDID_DAT_PCH	/Optimus 3	00hm	4 RN3507B	LVDS_EDID_DAT_C
DDC_DATA_PCH	/Optimus 7	00hm	8 RN3507D	VGA_DAT
DDC_CLK_PCH	/Optimus 5	00hm	6 RN3507C	VGA_CLK

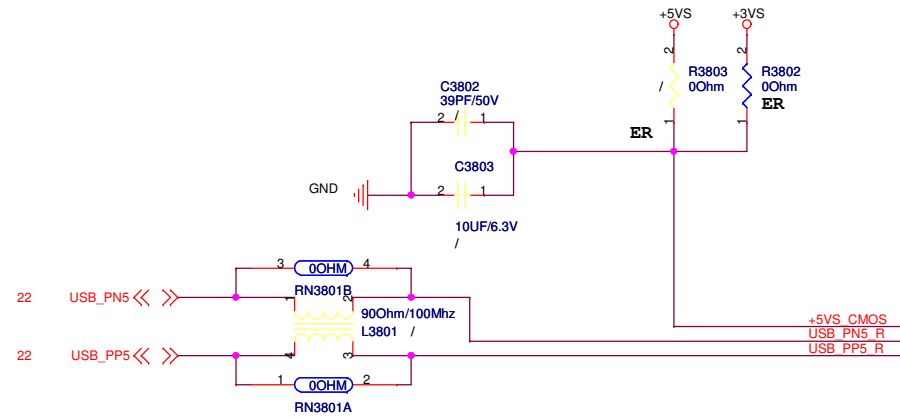


Support dGPU boot mode => Use DGPU_PWM_SELECT#

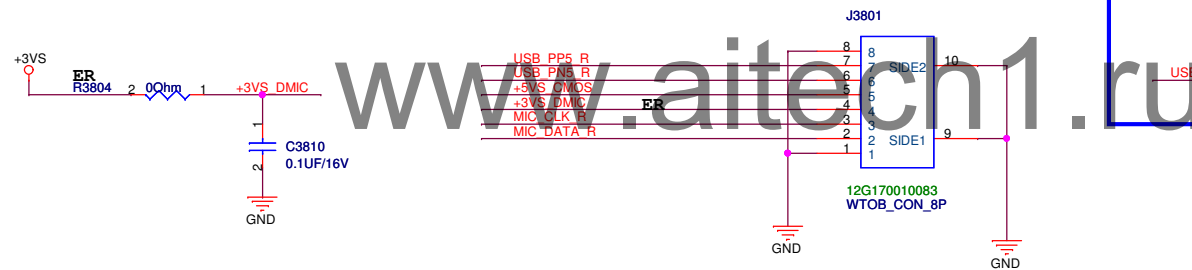
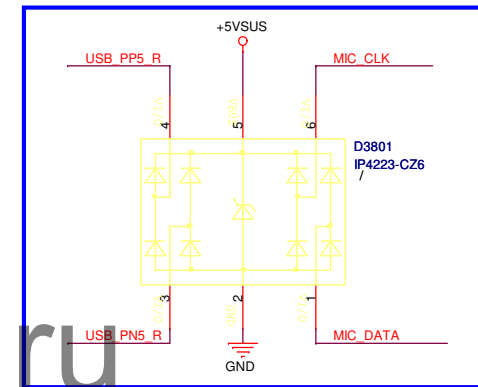


Camera Module & Mic.

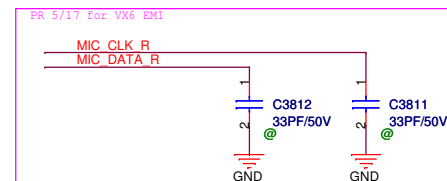
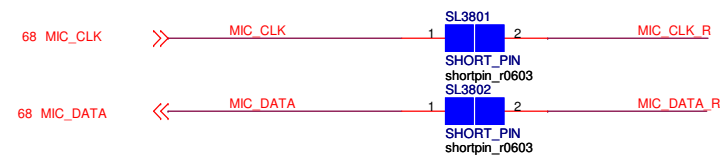
R4501 and R4502 depend on CMOS module support.



D6701 Close to J6701




Int DMIC

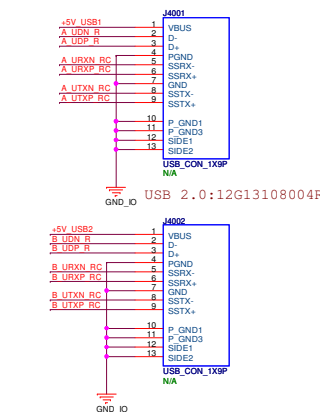
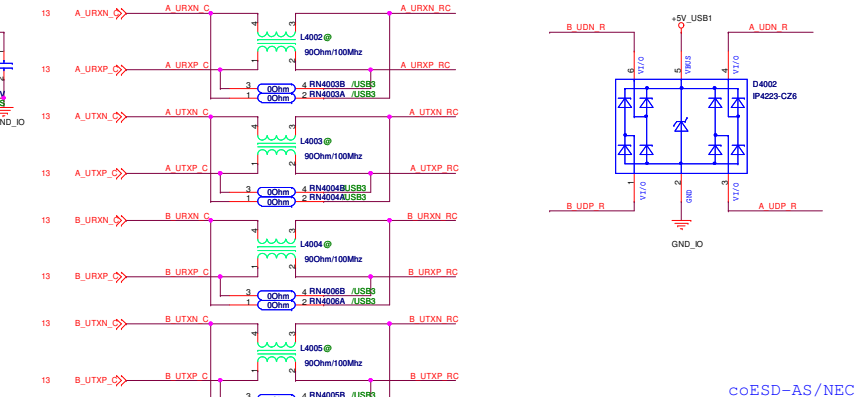
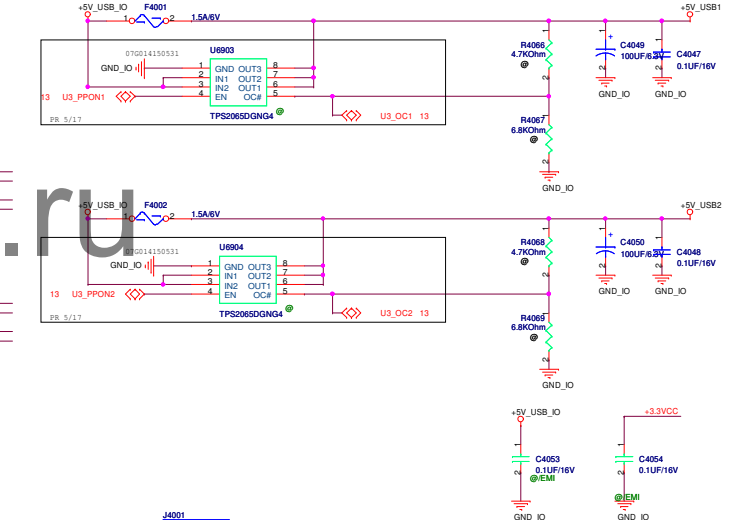
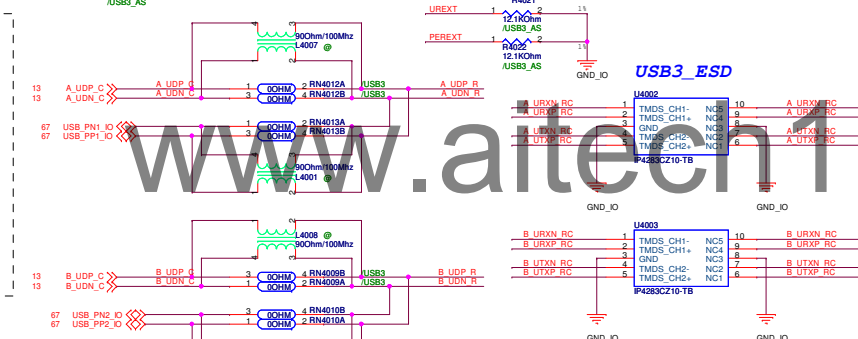
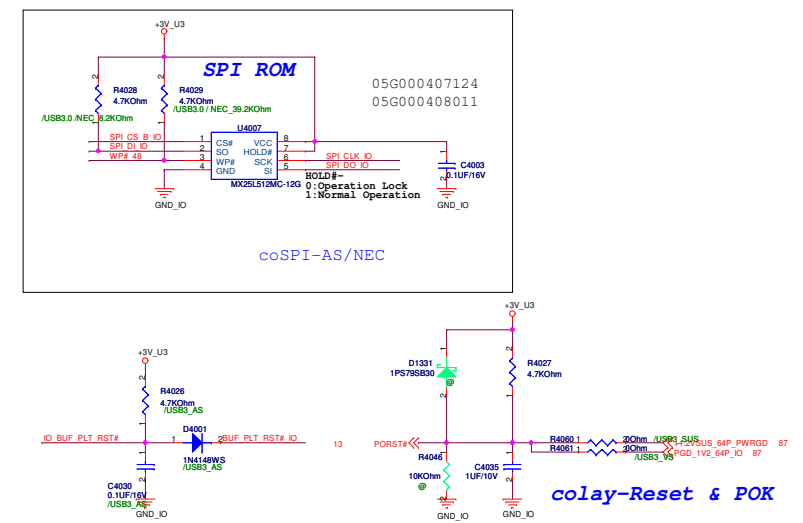


<Variant Name>

ASUS		Title : I/O, SPK, INT MIC, CMOS	
ASUSTeK COMPUTER INC		Engineer: Aries/Jesse	
Size B	Project Name 1215		Rev 1.0
Date: Monday, May 24, 2010		Sheet 38 of 97	


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<Variant Name>			
		Title : IO_USB3.0_1***	
ASUSTeK COMPUTER INC		Engineer: Aries/Jesse	
Size	Project Name		Rev
C	1215		1.0
Date: Monday, May 24, 2010		Sheet	39 of 97




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<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size A	Project Name UL20A		Rev 2.1
Date: Monday, May 24, 2010		Sheet	41 of 97

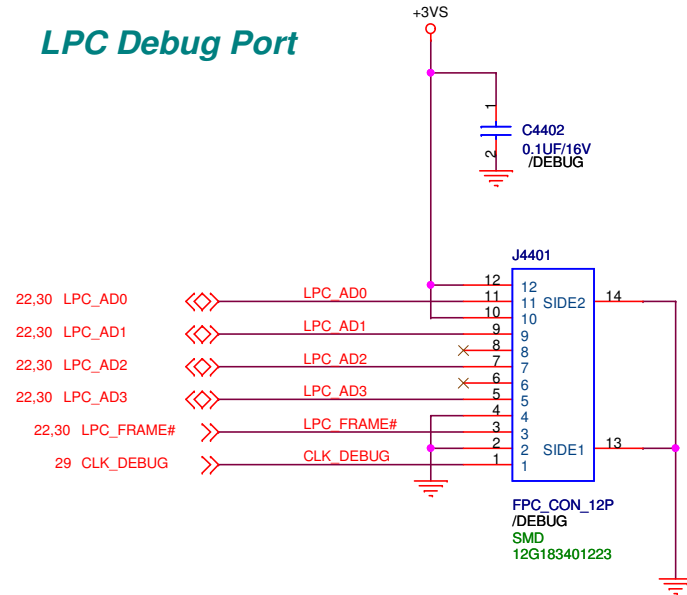
www.aitech1.ru

<Variant Name>

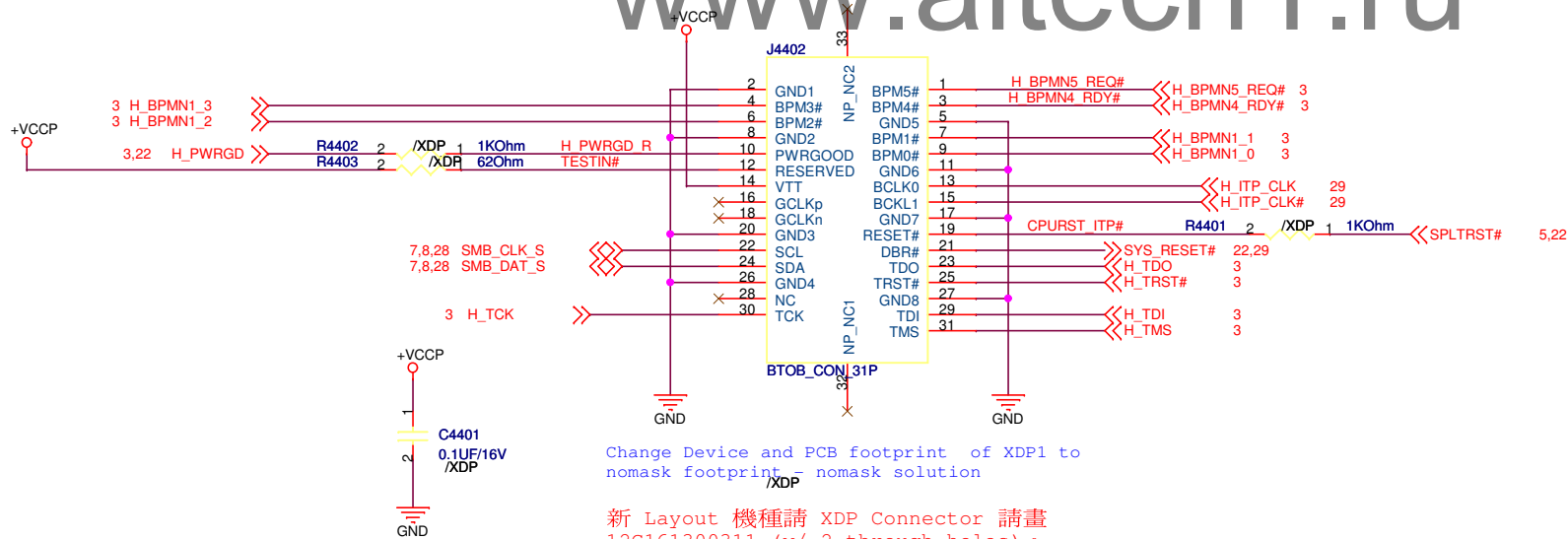
		Title : CB EXPRESS CARD CONN	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size A	Project Name UL20A		Rev 2.1
Date: Monday, May 24, 2010		Sheet	43 of 97

LPC DEBUG PORT

LPC Debug Port



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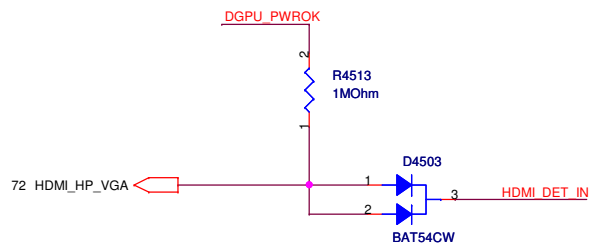
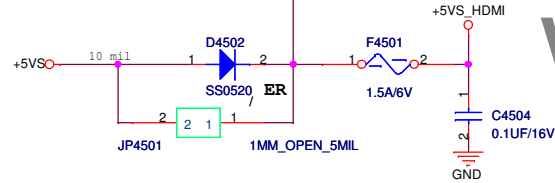
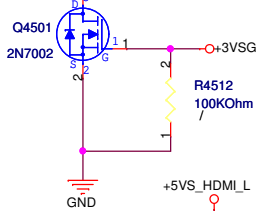
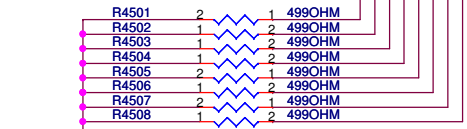
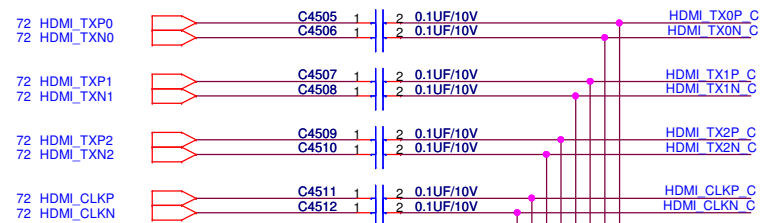


Change Device and PCB footprint of XDP1 to
nomask footprint - nomask solution

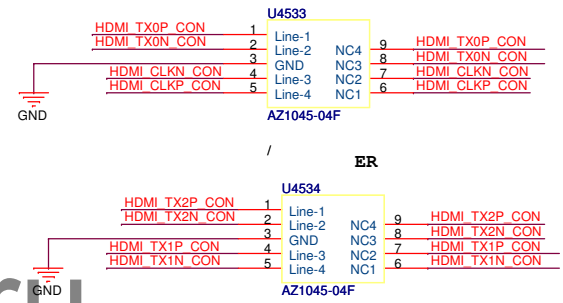
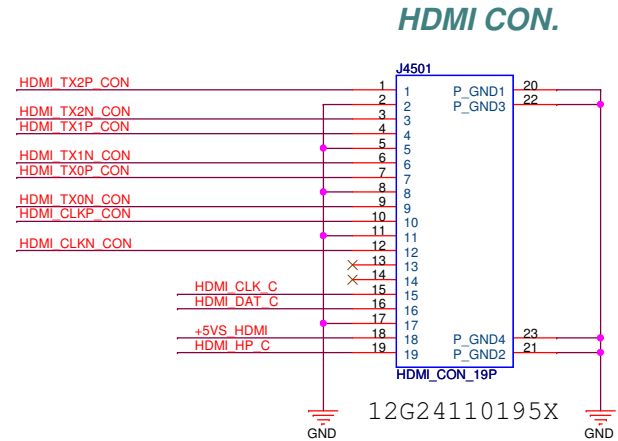
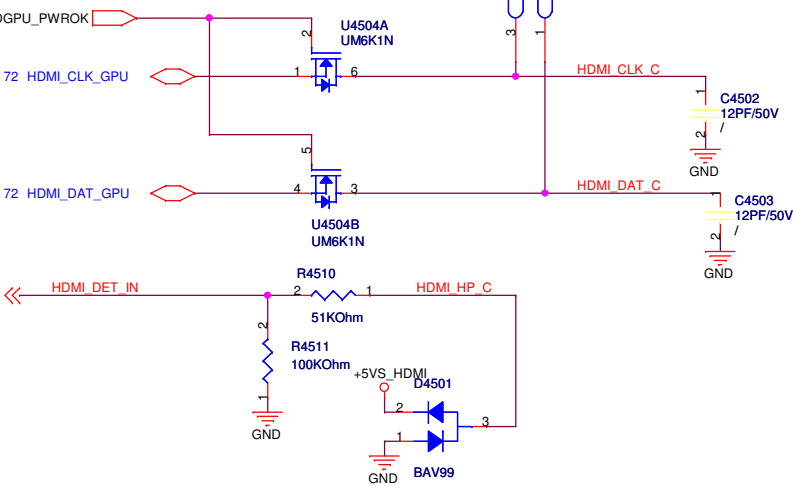
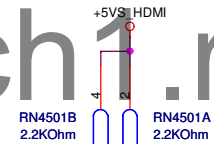
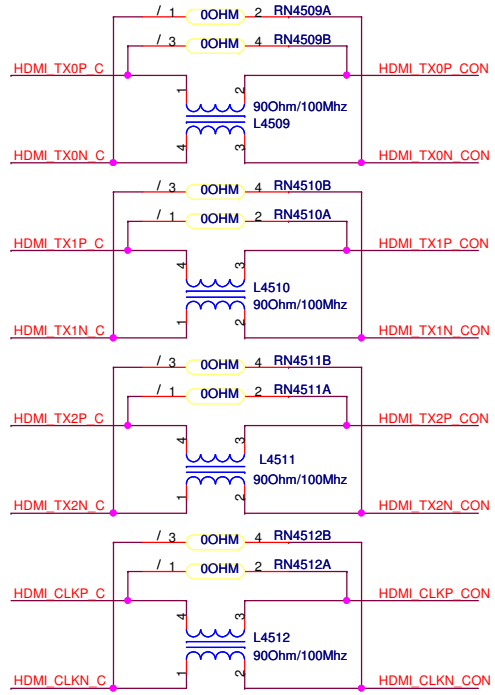
新 Layout 機種請 XDP Connector 請畫
12G161300311 (w/ 2 through holes)。

<Variant Name>

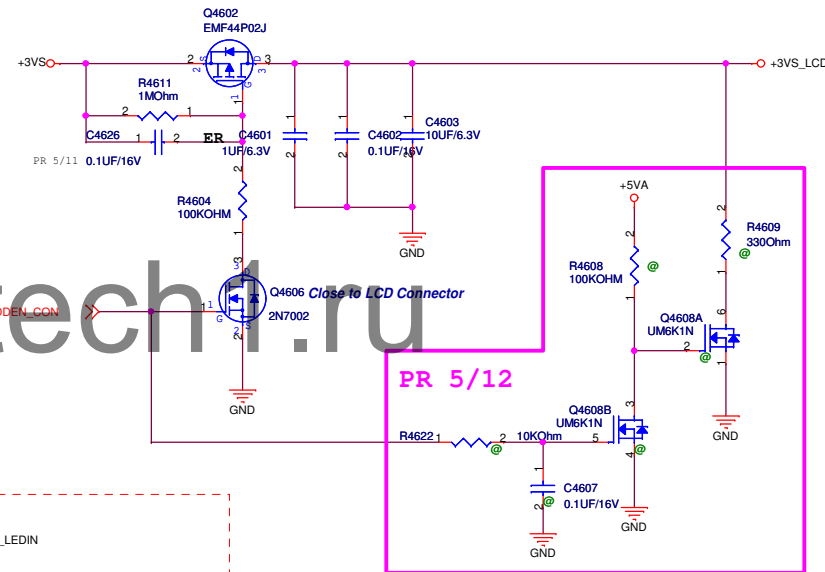
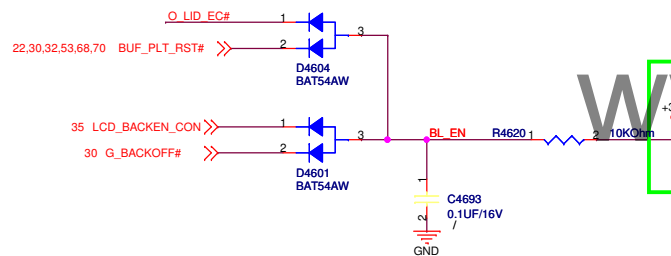
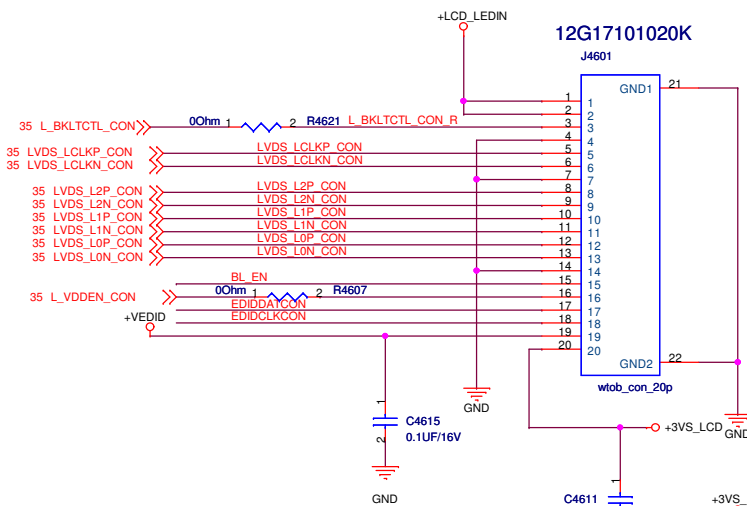
ASUS		Title : BUG DEBUG PORT	
ASUSTeK COMPUTER INC		Engineer: Aries/Jesse	
Size	Project Name	1215	Rev
Custom			1.0
Date: Monday, May 24, 2010		Sheet	44 of 97



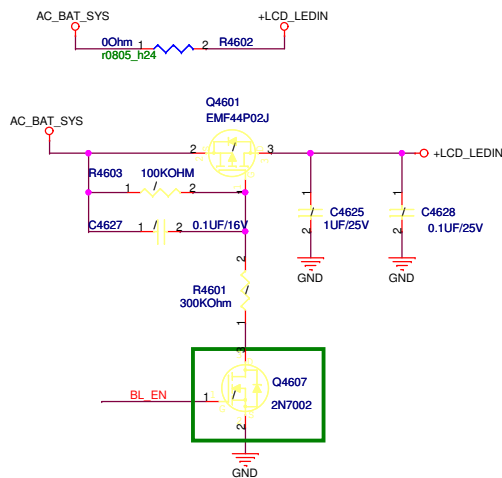
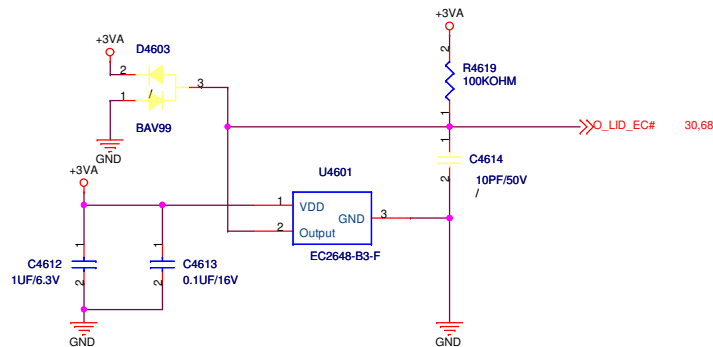
www.aitech1.ru



ASUS		Title : HDMI_CONN	
ASUSTeK COMPUTER INC. NB4		Engineer: Aries/Jesse	
Size B	Project Name 1215	Rev 1.00	
Date: Monday, May 24, 2010		Sheet 45 of 97	

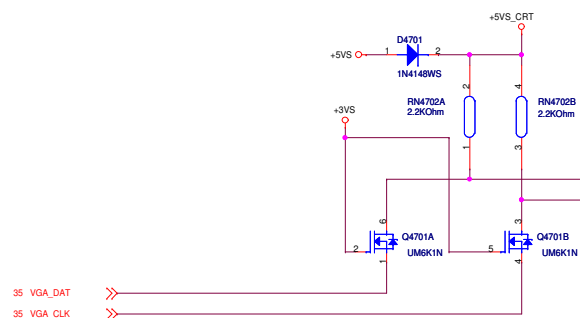
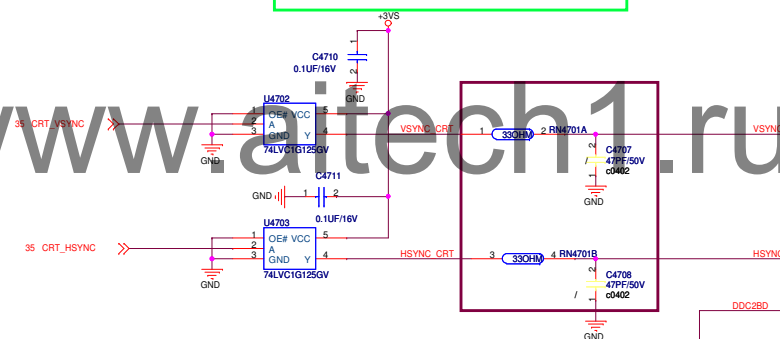
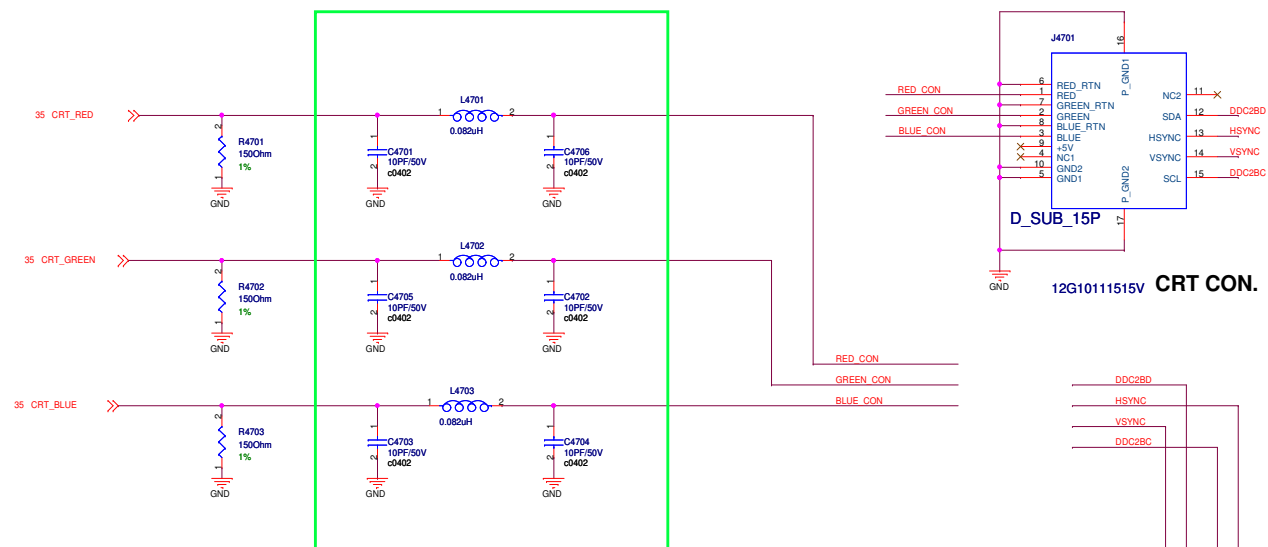
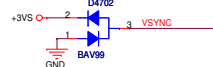
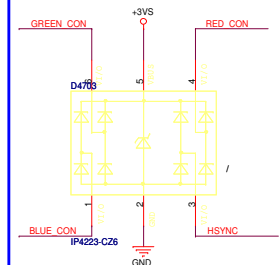


Backlight Enable Discharge




<Variant Name>

ASUS		Title : LVDS Conn	
ASUSTek Computer INC.		Engineer: Aries/Jesse	
Size Custom	Project Name 1215	Rev 1.0	
Date: Monday, May 24, 2010		Sheet 46 of 97	




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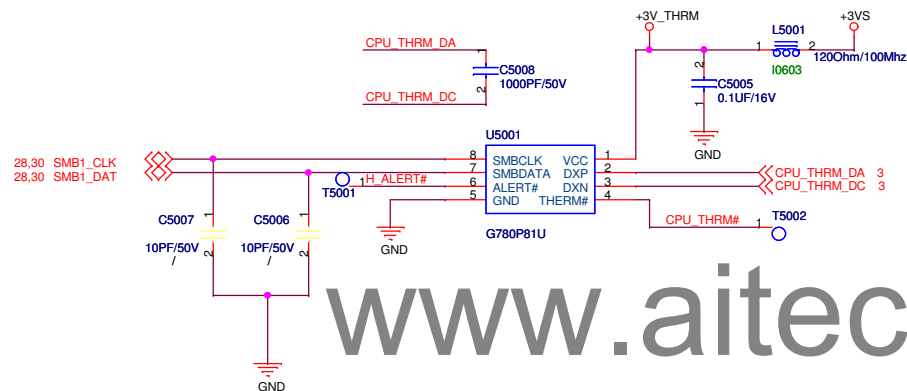
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name		Rev
<i>A</i>	<i>UL20A</i>		<i>2.1</i>
Date: <i>Monday, May 24, 2010</i>		Sheet	48 of 97

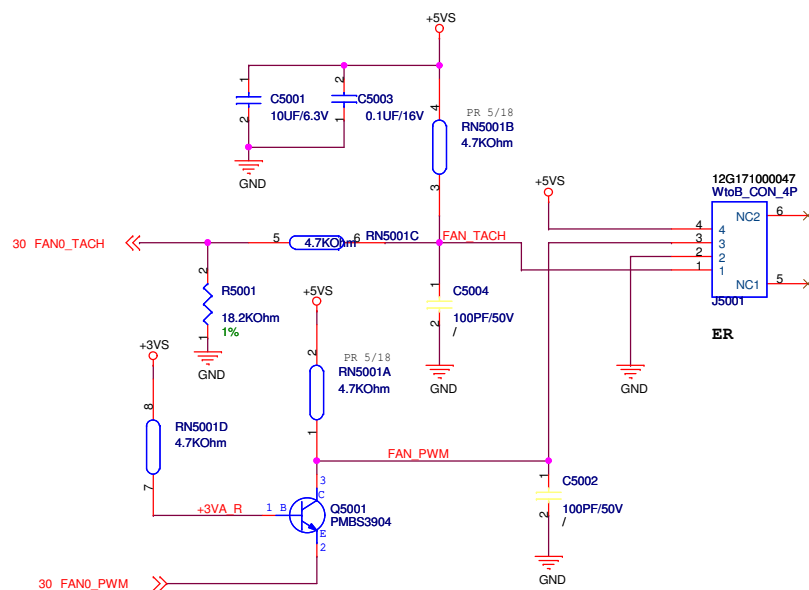
www.aitech1.ru

<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name		Rev
<i>A</i>	<i>UL20A</i>		<i>2.1</i>
Date: <i>Monday, May 24, 2010</i>		Sheet	49 of 97



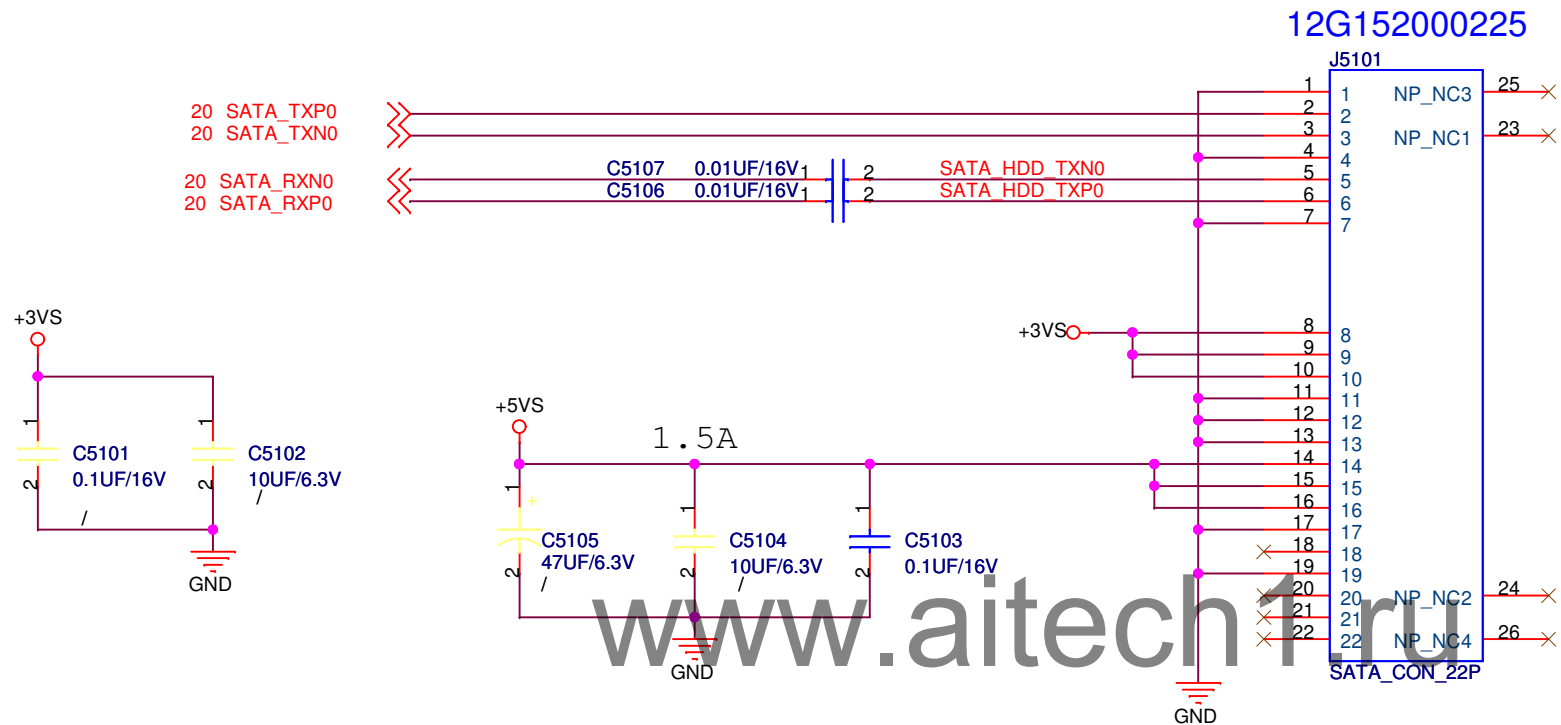
FAN CONN



<Variant Name>

ASUS		FAN THERMAL SENSOR FAN CONN	
ASUSTeK COMPUTER INC		Engineer: Aries/Jesse	
Size	Project Name	1215	Rev 1.0
Custom			
Date: Monday, May 24, 2010	Sheet	50	of 97

SATA HDD



<Variant Name>



Title: XDD SATA HDD CONN

ASUSTeK COMPUTER INC

Engineer: Aries/Jesse

Size
A

Project Name
1215

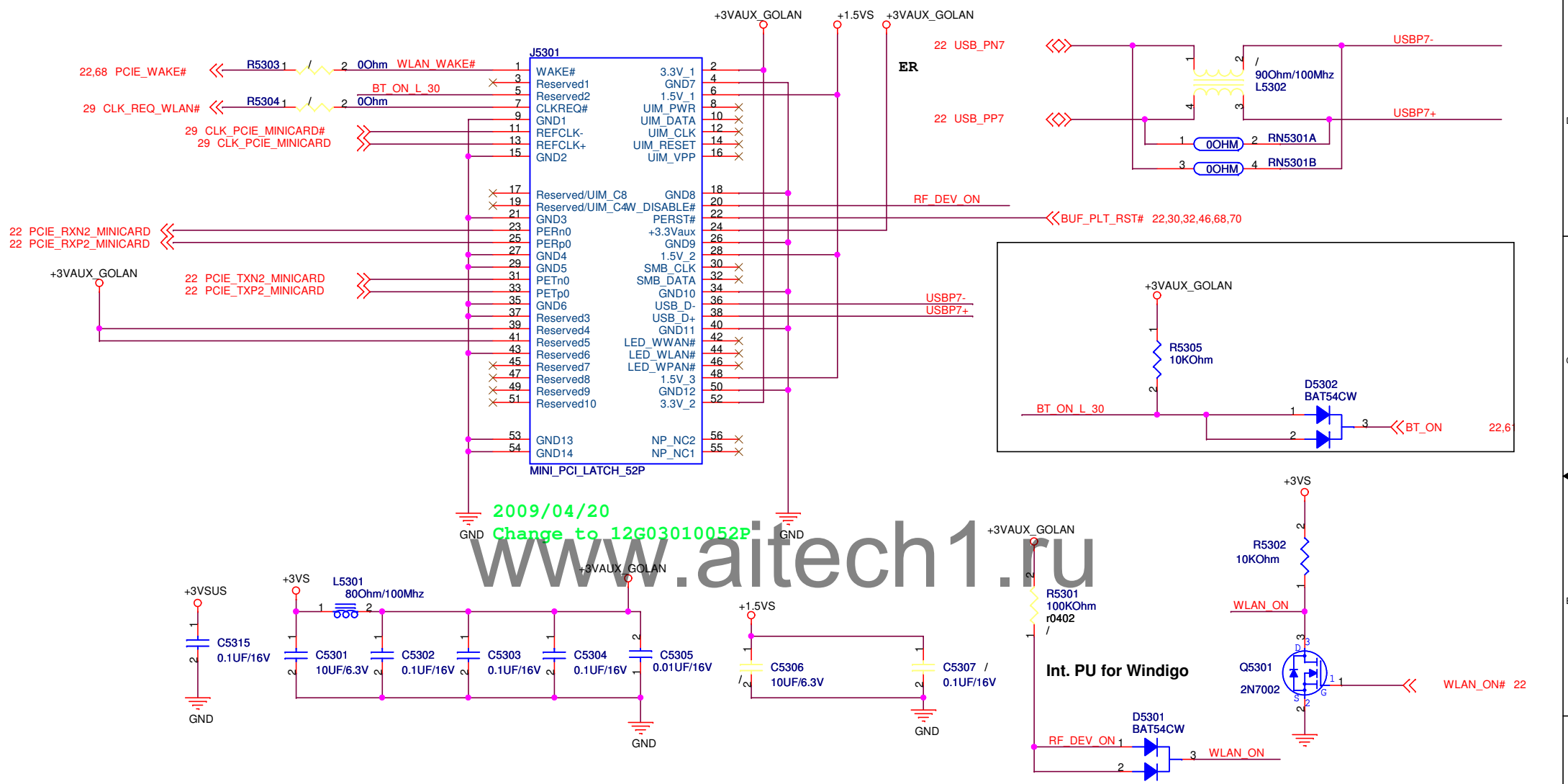
Rev
1.0

Date: Monday, May 24, 2010

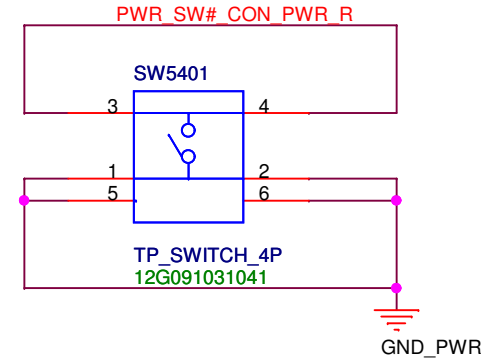
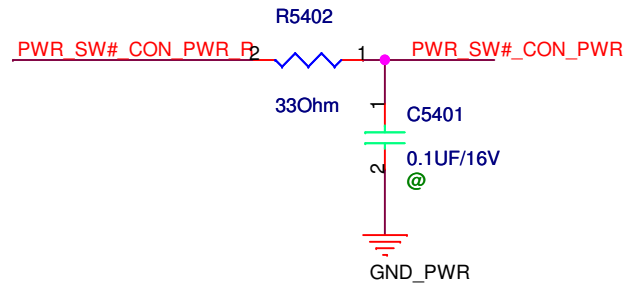
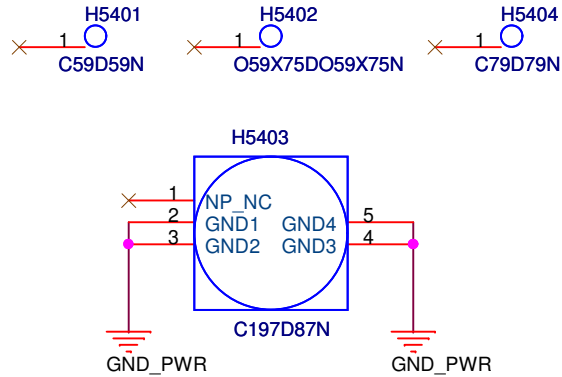
Sheet 51 of 97



INPUT					OUTPUT	
OE#	MS	PE#	SB#	SEL	INT	D+/D-
0	0	X	0	0	Hi-Z	Short
0	1	0	0	X	H	Auto

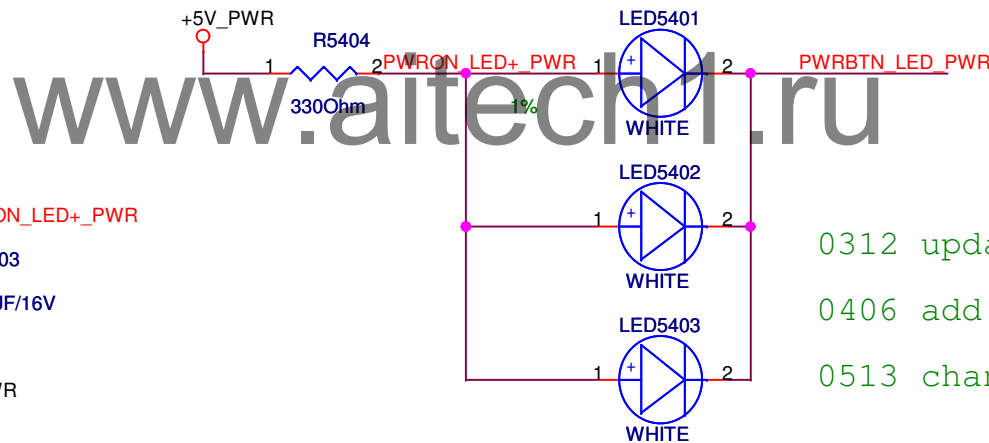
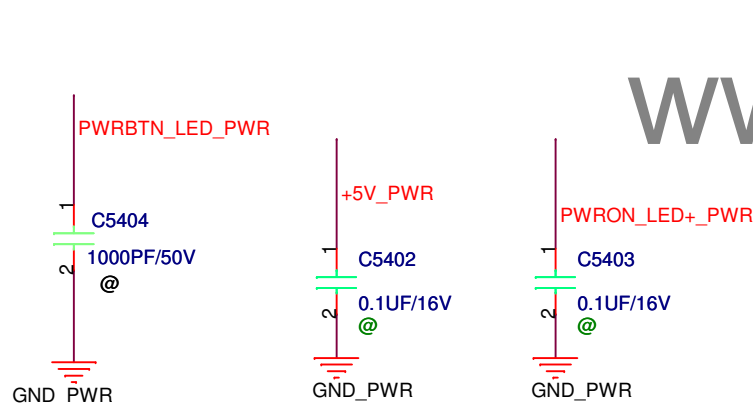


PWR SW

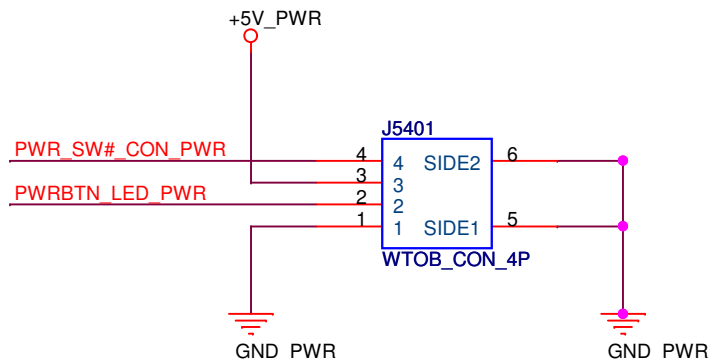


0510 revised hole

For POWER ON LED

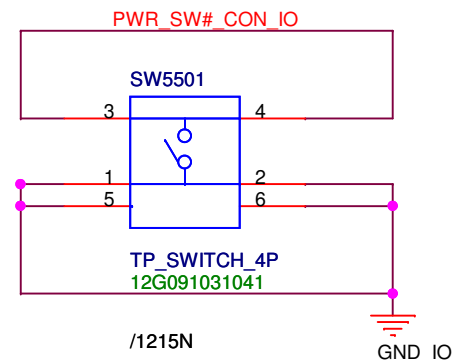
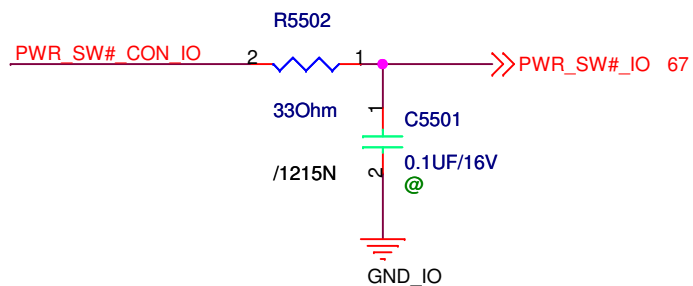


0312 update LED to 0603
0406 add LED*3 (anderson)
0513 change white LED

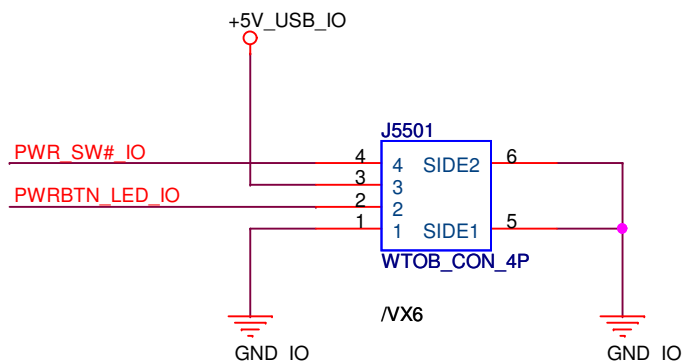
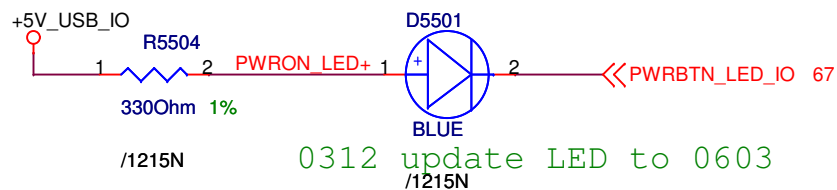


ASUS		Title : PWR_BUTTON_LED	
ASUSTEK COMPUTER INC		Engineer: Shangyu/Anderson	
Size A	Project Name VX6_PWR_BTN		Rev 1.3
Date: Monday, May 24, 2010		Sheet 54 of 97	

PWR SW



For POWER ON LED



ASUS		Title :PWR_BUTTON_LED	
ASUSTEK COMPUTER INC		Engineer: Anndy_wang	
Size A	Project Name 1005P_IO		Rev 1.3
Date: Monday, May 24, 2010		Sheet 55 of 97	

The schematic diagram illustrates the ER evaluation board, which is a 12G183301208 board. It features several key components and connections:

- Power Section:** A +5V power source is connected to the board via a SL5601 connector. The power is distributed to various components, including a C5601 capacitor (1uF/16V) and a C5602 capacitor (0.1uF/16V). A +5V_TP test point is also shown.
- Control Section:** The board includes a TP_CLK and TP_DAT test points, which are connected to the board's control lines. A C5603 capacitor (33pF/50V) is connected to the TP_CLK line, and a C5604 capacitor (33pF/50V) is connected to the TP_DAT line.
- Data Section:** The board has a 12G091031041 data connector. The data lines are connected to the board's data pins, which are labeled 1 through 12. The data lines are also connected to the board's data pins, which are labeled 1 through 12.
- Switches:** The board includes two switches, SW5602 and SW5601, which are used to select between different data sources. The switches are connected to the board's data pins, which are labeled 1 through 12.
- Other Components:** The board includes a C5601 capacitor (1uF/16V), a C5602 capacitor (0.1uF/16V), a C5603 capacitor (33pF/50V), and a C5604 capacitor (33pF/50V).

For CHARGE LED

LED5604
ORANGE
GREEN
GREEN(ORANGE)
07G015700738

+3V5US

3 2 1 2 1 2

CHG_LED_ORANGE#

CHG_LED_GREEN#

R5604
330Ohm
1% /1215N

R5605
330Ohm
1% /1215N

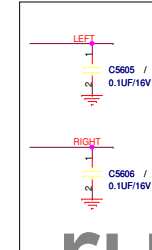
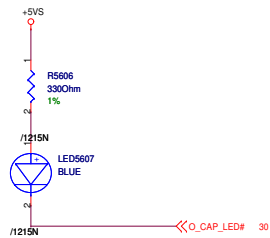
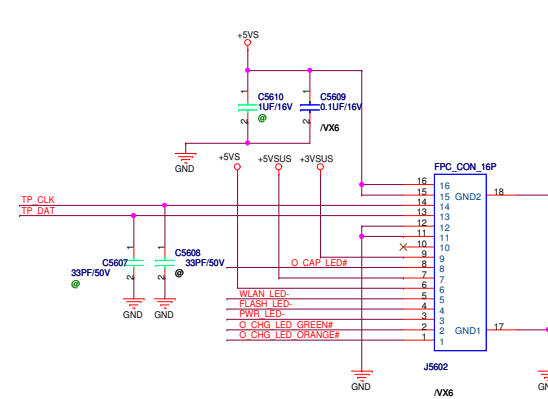
30 CHG_FULL_LED#

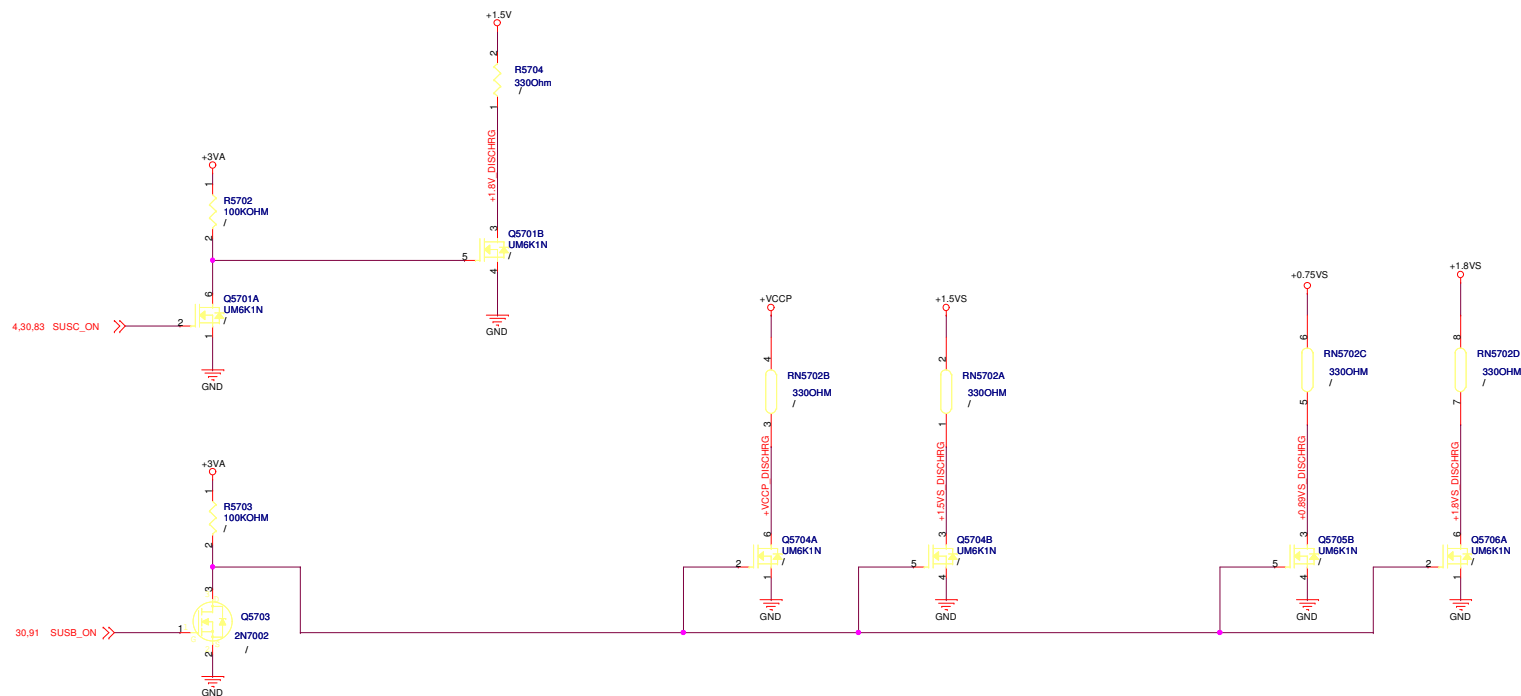
30 CHG_LED#

O CHG_LED_GREEN#

O CHG_LED_ORANGE#

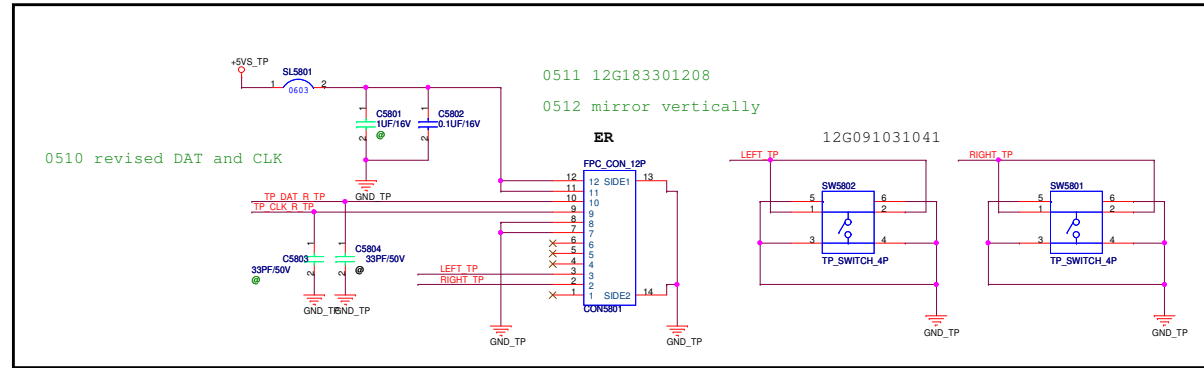
/1215N





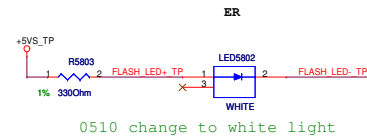
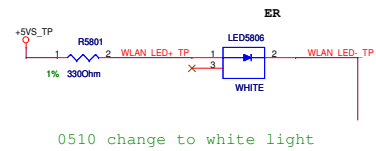
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Touch-Pad Conn. Right/Left SW.

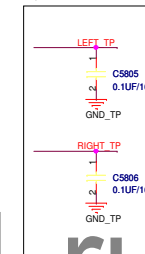


For IDE/FLASH LED

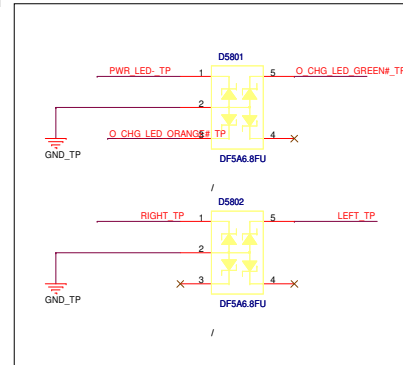
For WLAN LED



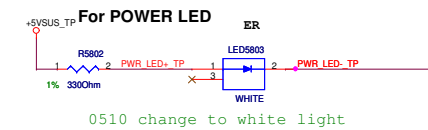
6/30 EMI near BTN



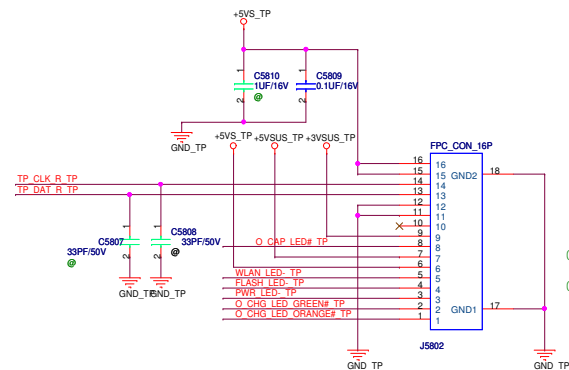
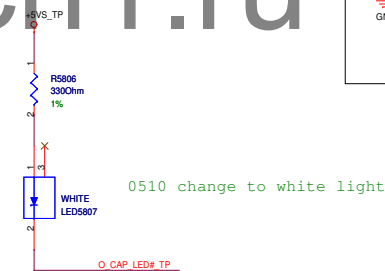
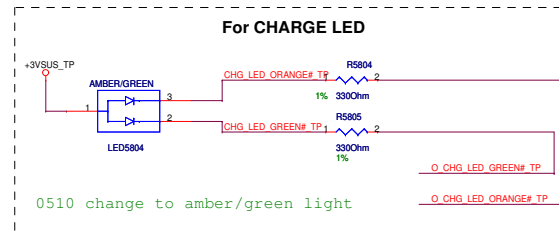
6/22 for ESD



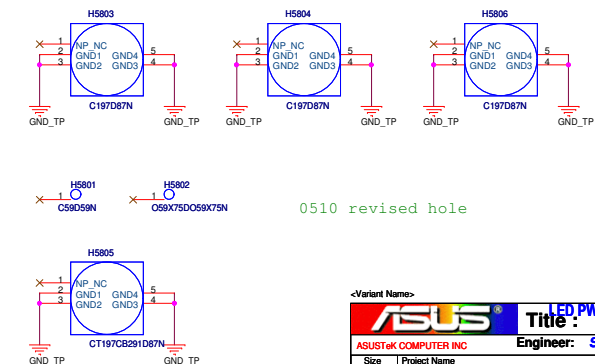
PWR LED



Charge LED




0406 mirror vertically (anderson)
0510 mirror vertically for positive/negative line



0510 revised hole

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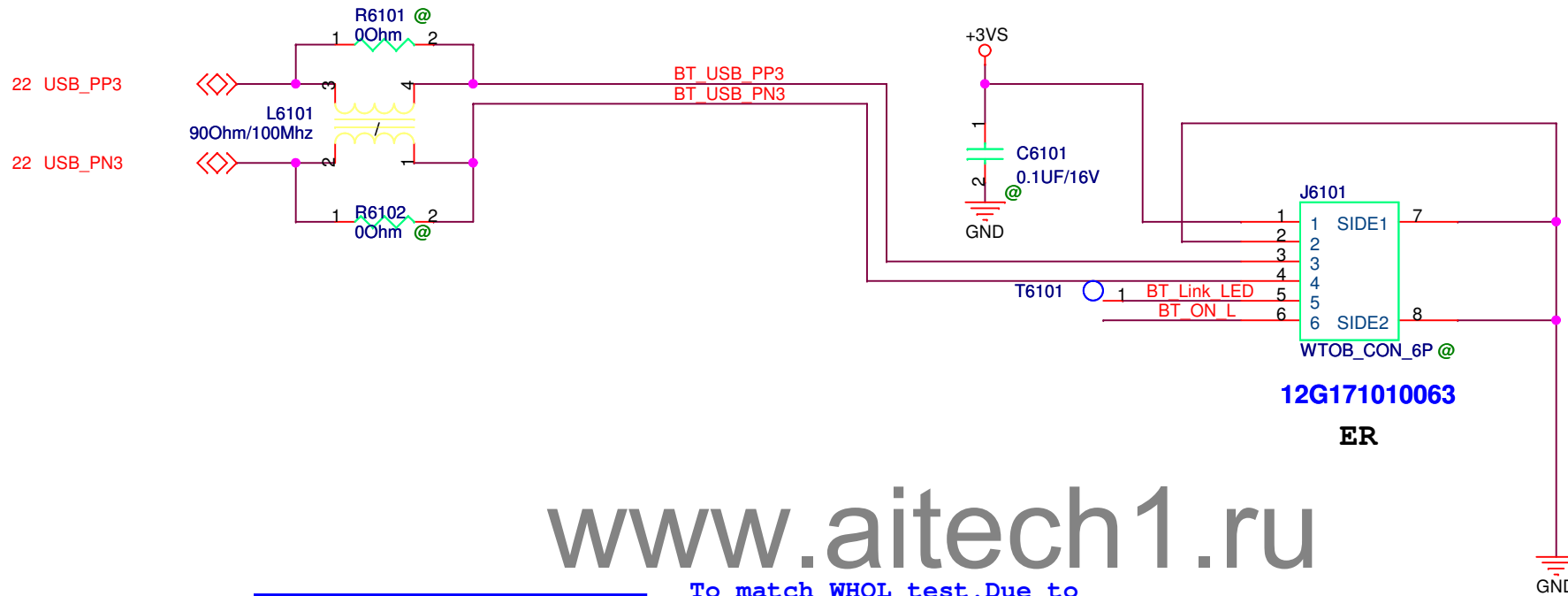
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size	Project Name		Rev
<i>A</i>	<i>UL20A</i>		<i>2.1</i>
Date: <i>Monday, May 24, 2010</i>		Sheet	59 of 97

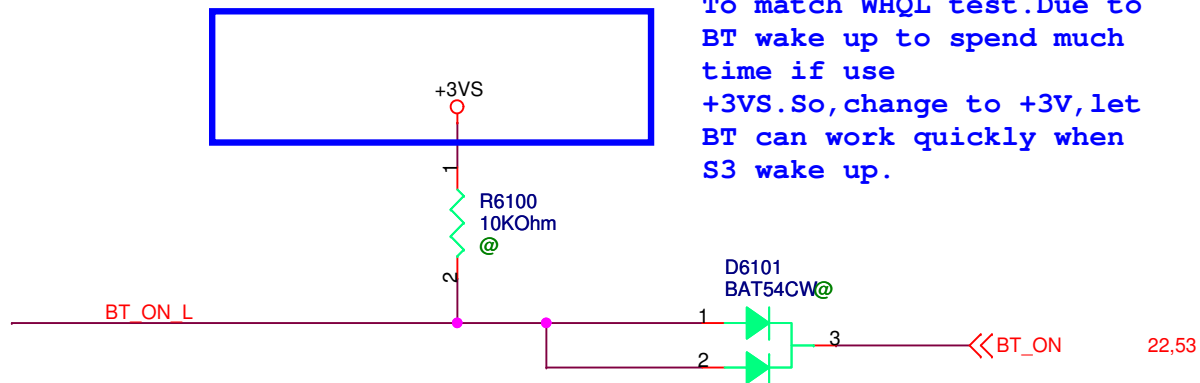
[illegible]

081111 -> 090604:
1. Change D6005 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.

BLUETOOTH CONNECTOR



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To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

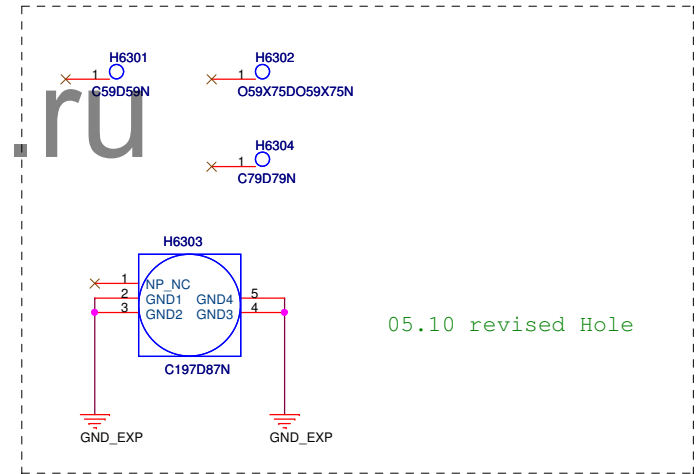
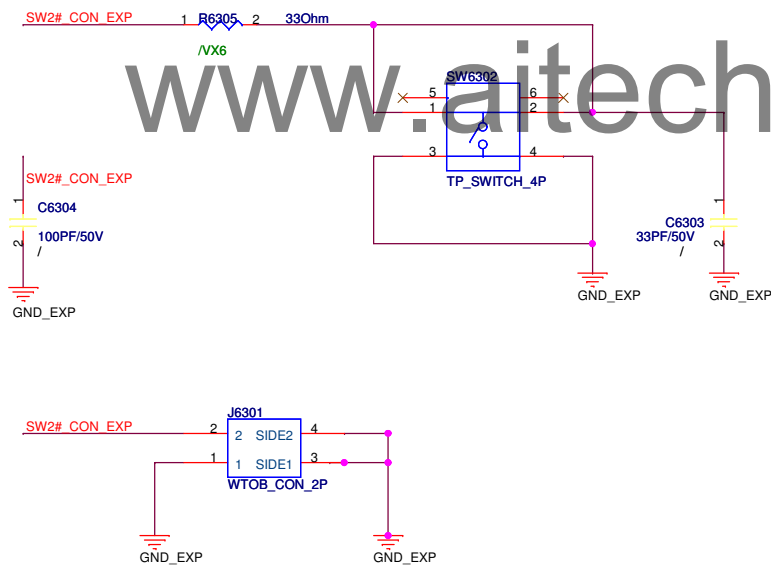
		Title : Blue Tooth	
ASUSTeK COMPUTER INC		Engineer: Aries/Jesse	
Size Custom	Project Name 1215		Rev 1.0
Date: Monday, May 24, 2010		Sheet 61 of 97	

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<Variant Name>

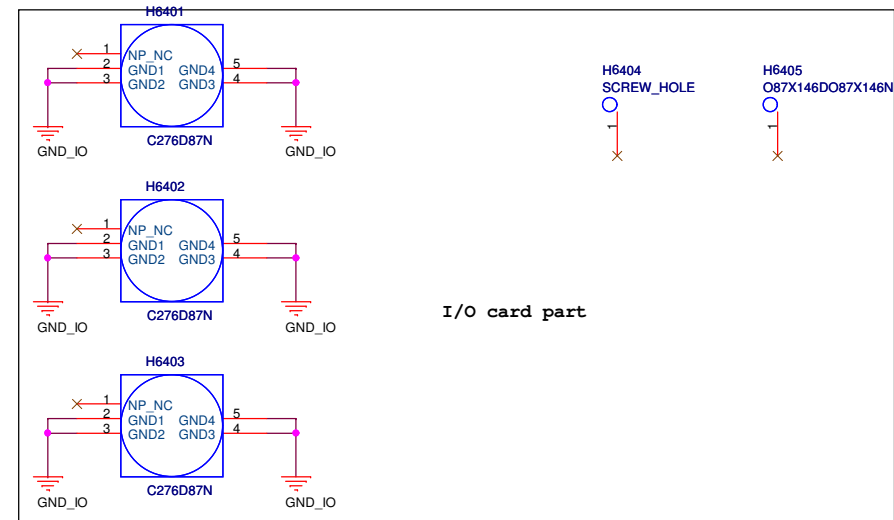
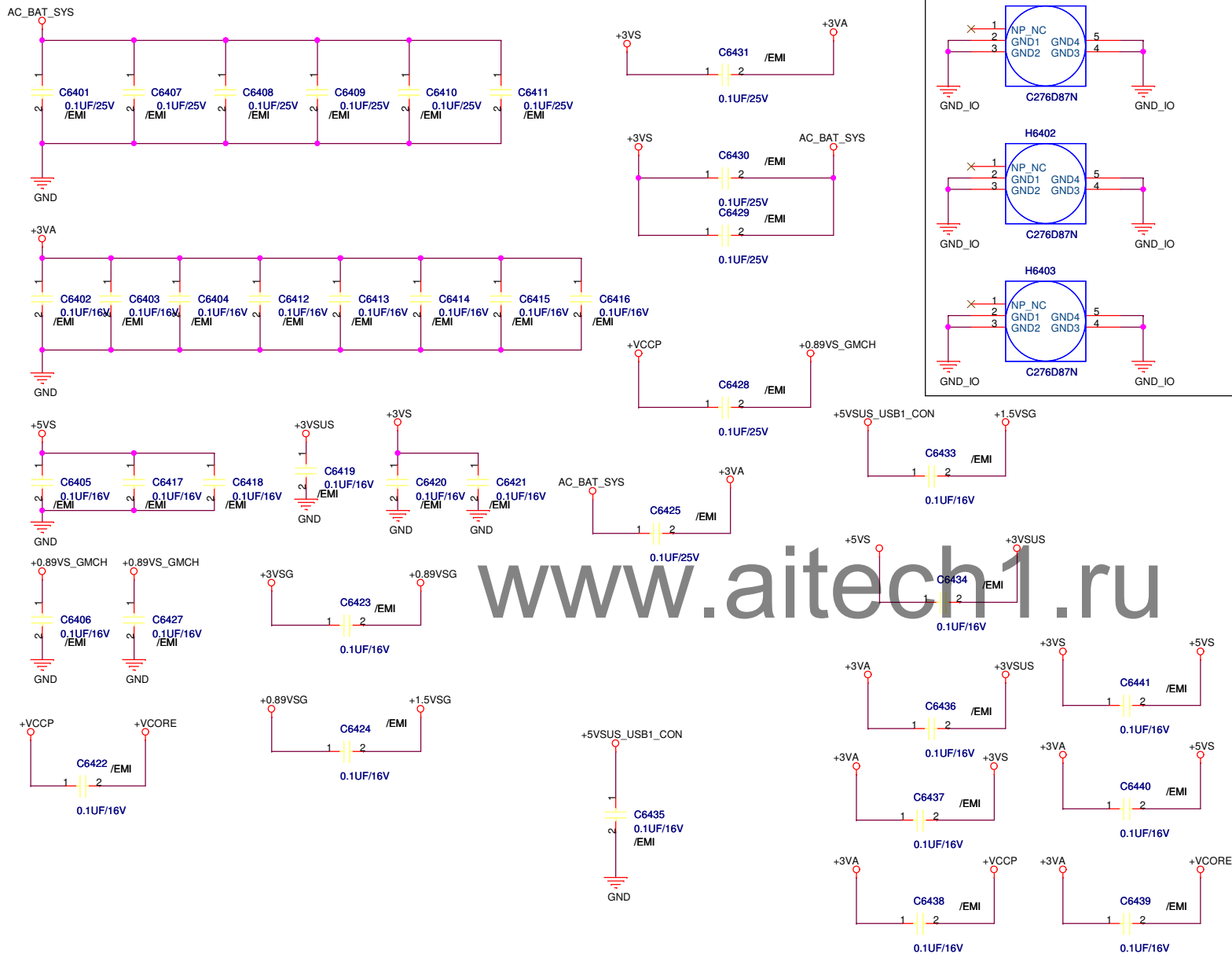
		Title : TPM	
ASUSTeK COMPUTER INC		Engineer: Jerry Yu	
Size A	Project Name UL20A		Rev 2.1
Date: Monday, May 24, 2010		Sheet	62 of 97

Express gate



05.10 revised Hole

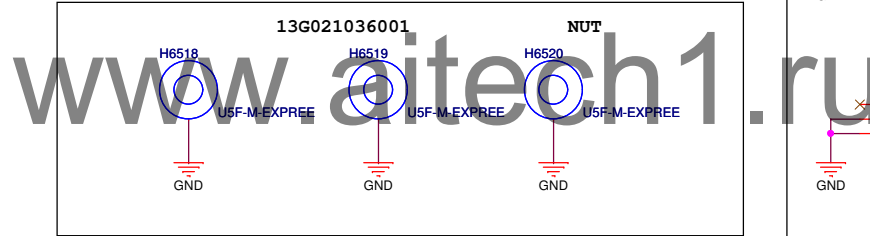
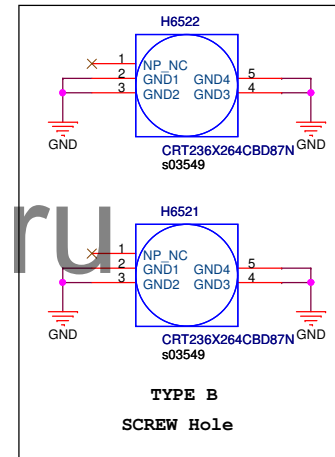
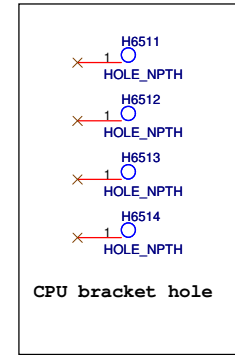
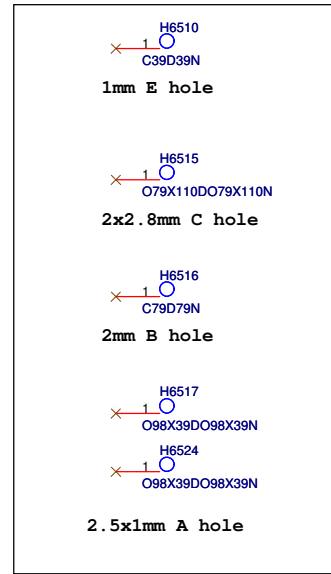
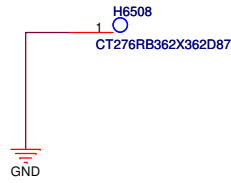
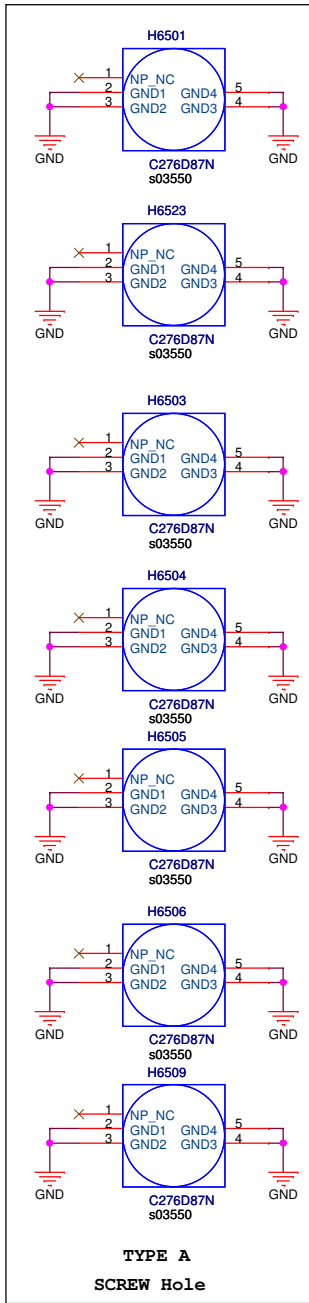
<Variant Name>		Title :	
CMOS CMOS CAMERA		ASUSTeK COMPUTER INC	
Size		Project Name	
B		VX6_EXP	
Date: Monday, May 24, 2010		Sheet 63 of 97	
Rev		1.0	



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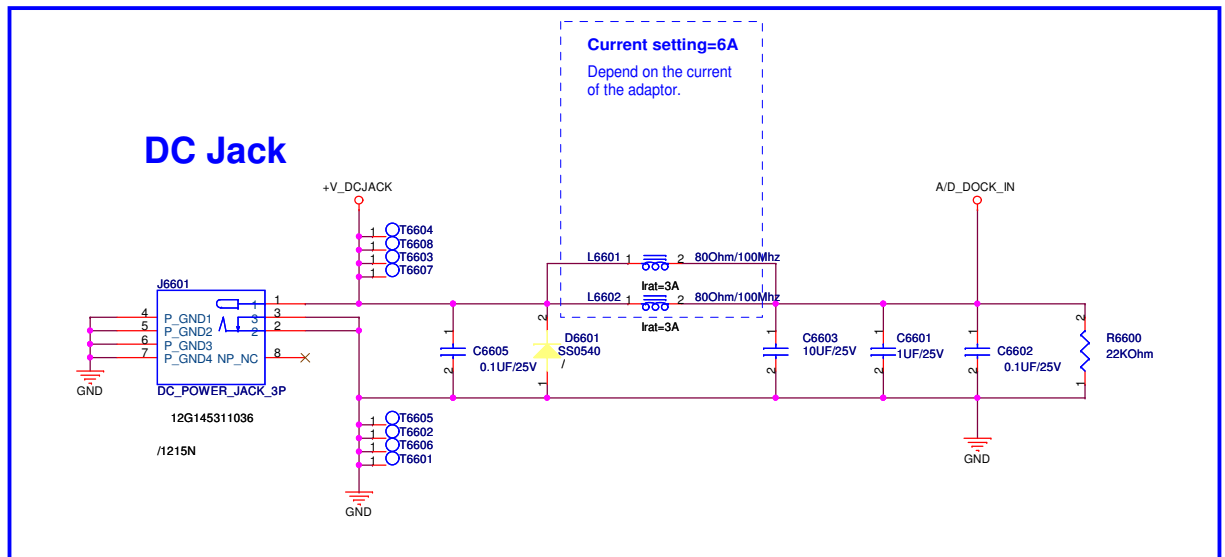
<Variant Name>

ASUS		Title : EMI_CAP	
ASUSTeK COMPUTER INC		Engineer: Aries/Jesse	
Size B	Project Name 1215	Rev 1.0	
Date: Monday, May 24, 2010		Sheet 64 of 97	

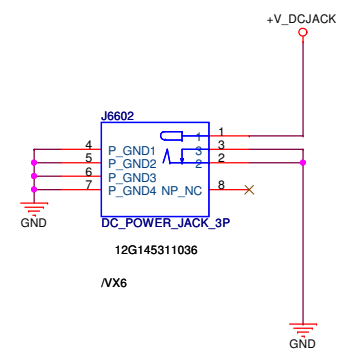


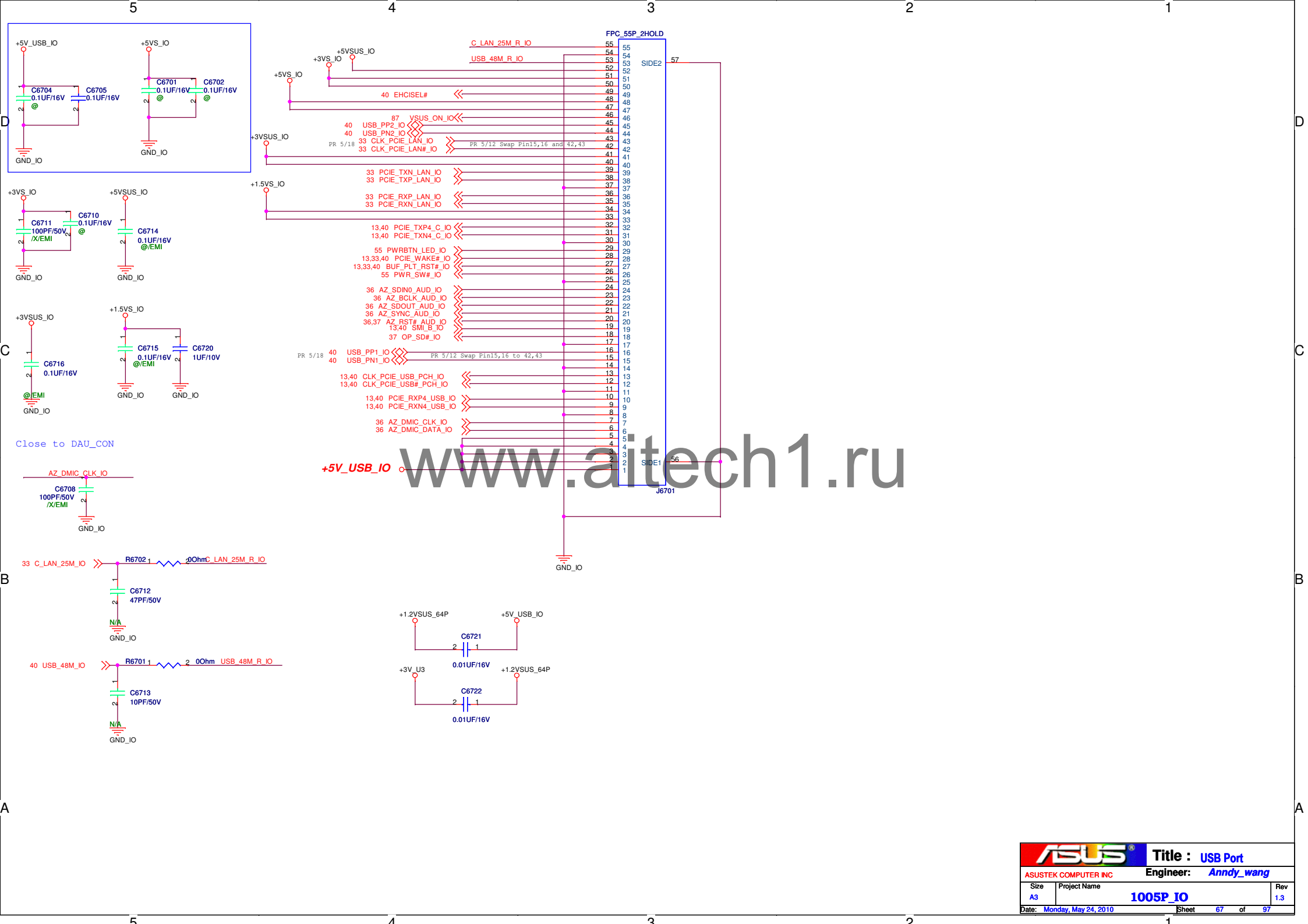
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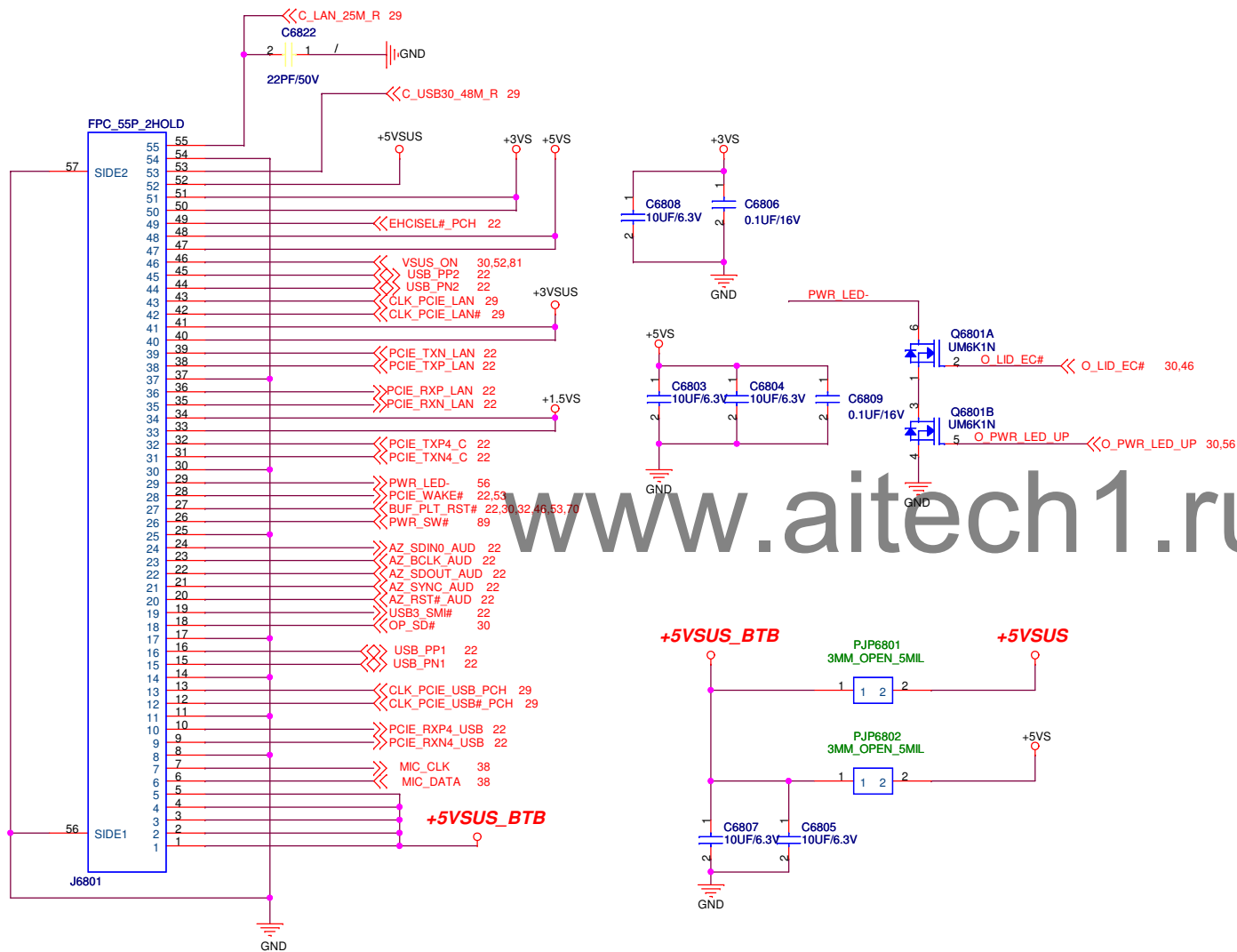
ASUS		Title : Srew Hole	
ASUSTek Computer INC.		Engineer: Aries/Jesse	
Size B	Project Name 1215		Rev 1.0
Date: Monday, May 24, 2010		Sheet 65 of 97	



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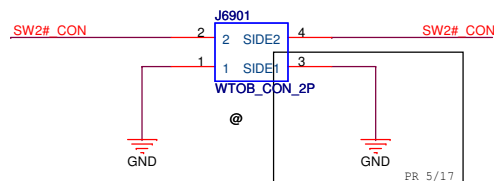
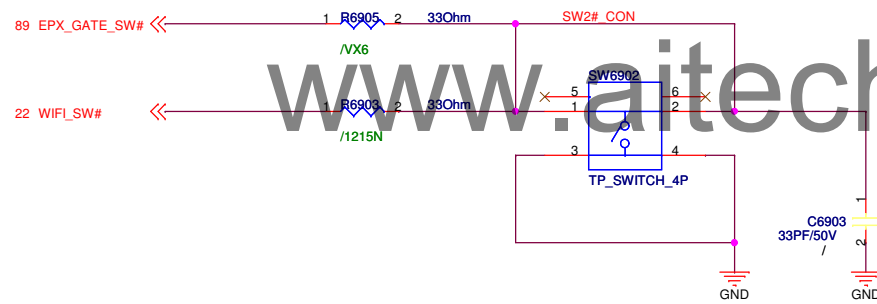
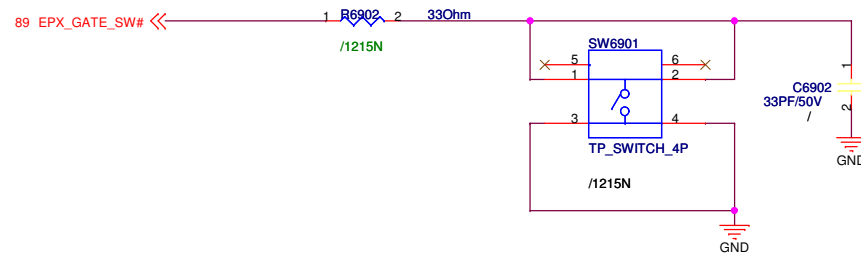




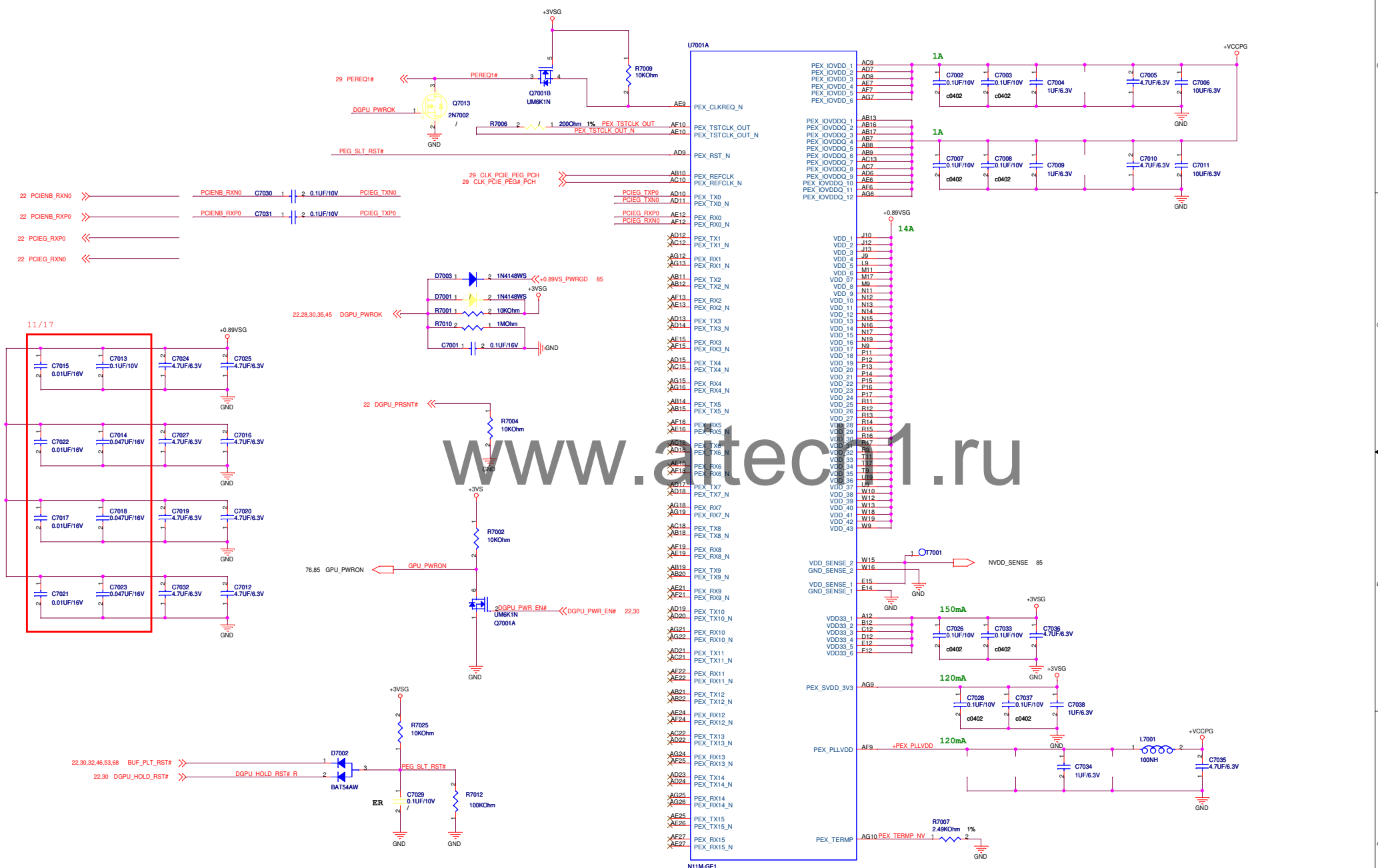


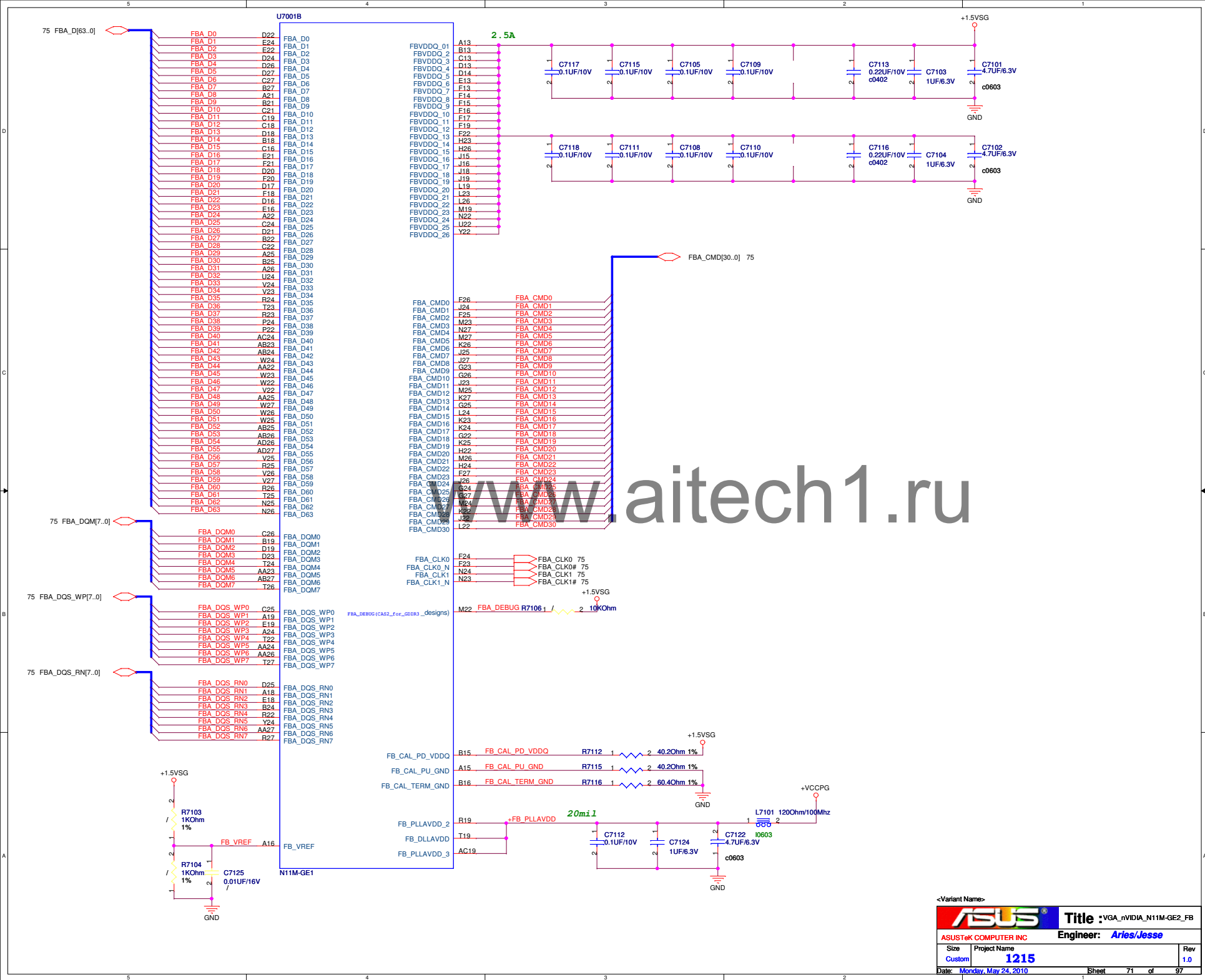
<Variant Name>

ASUS		Title : B TO B CONN	
ASUSTeK COMPUTER INC		Engineer: Arlee/Jesse	
Size B	Project Name 1215		Rev 1.0
Date: Monday, May 24, 2010		Sheet 68 of 97	

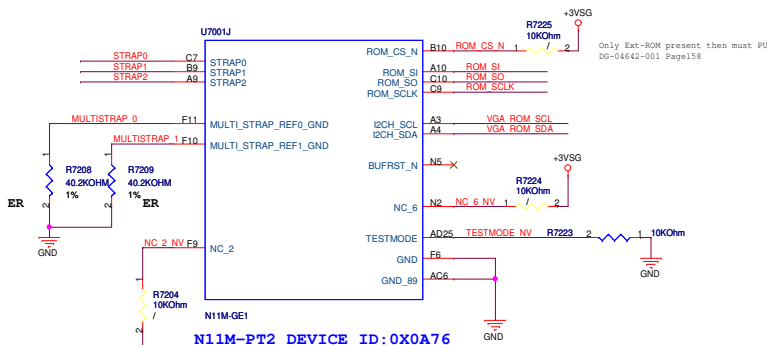
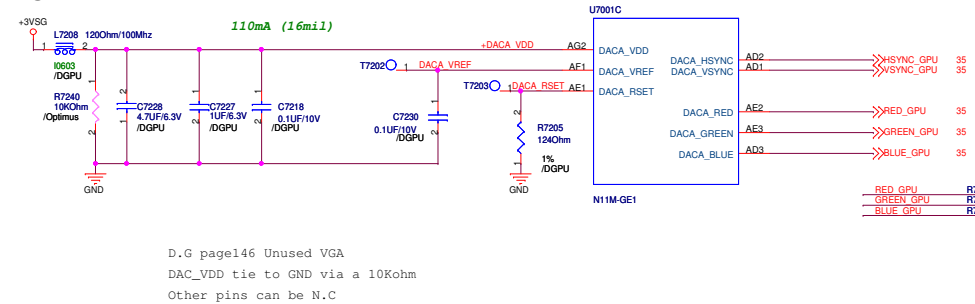


<Variant Name>		Title :	
CMOS CMOS CAMERA		ASUS	
ASUSTeK COMPUTER INC		Engineer: Aries/Jesse	
Size	Project Name	Rev	
B	1215	1.0	
Date: Monday, May 24, 2010		Sheet	69 of 97

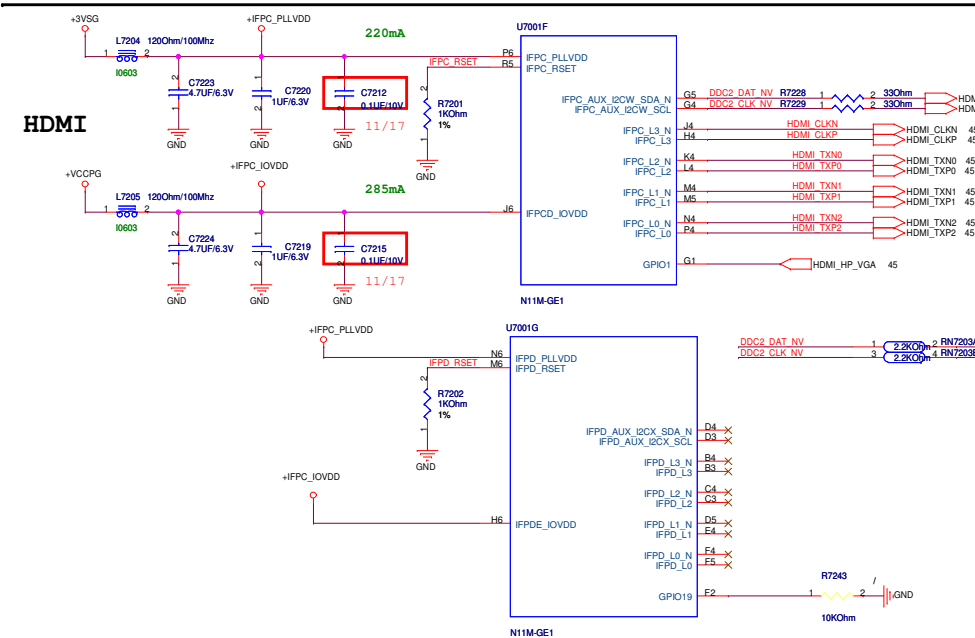
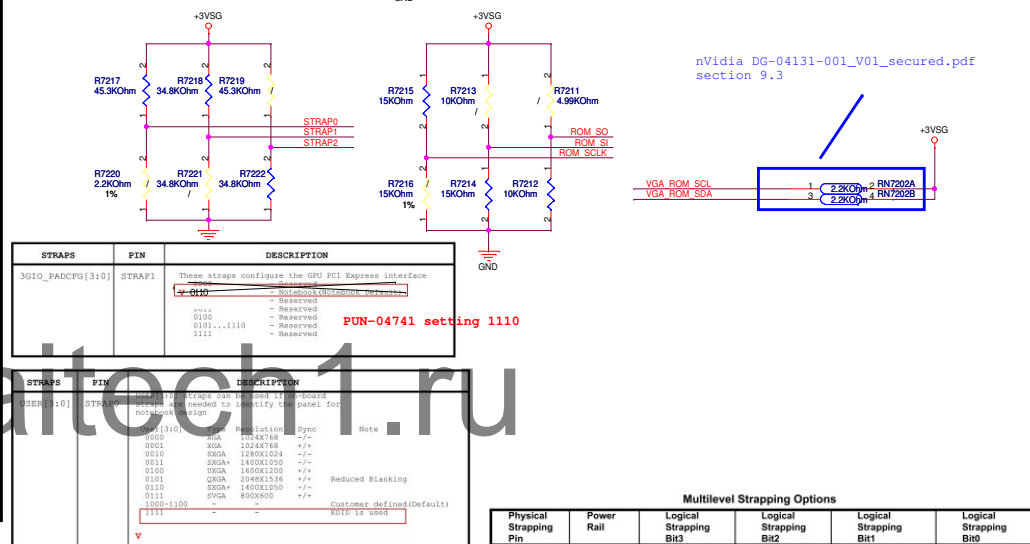
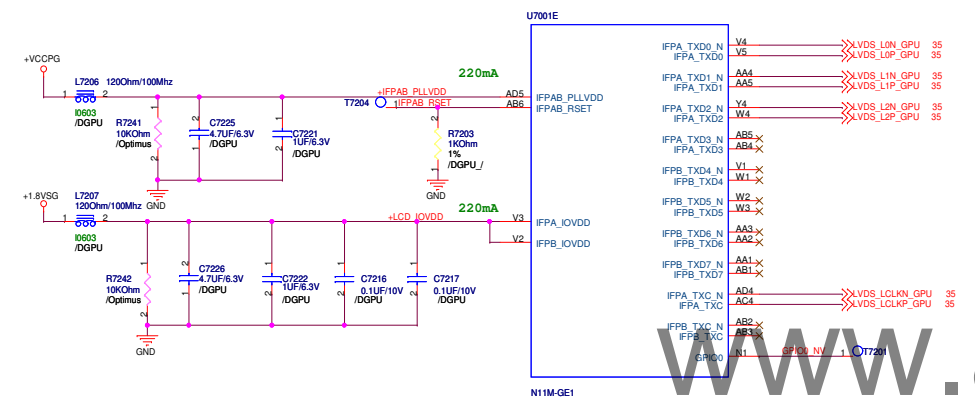




VGA



LVDS

[illegible]

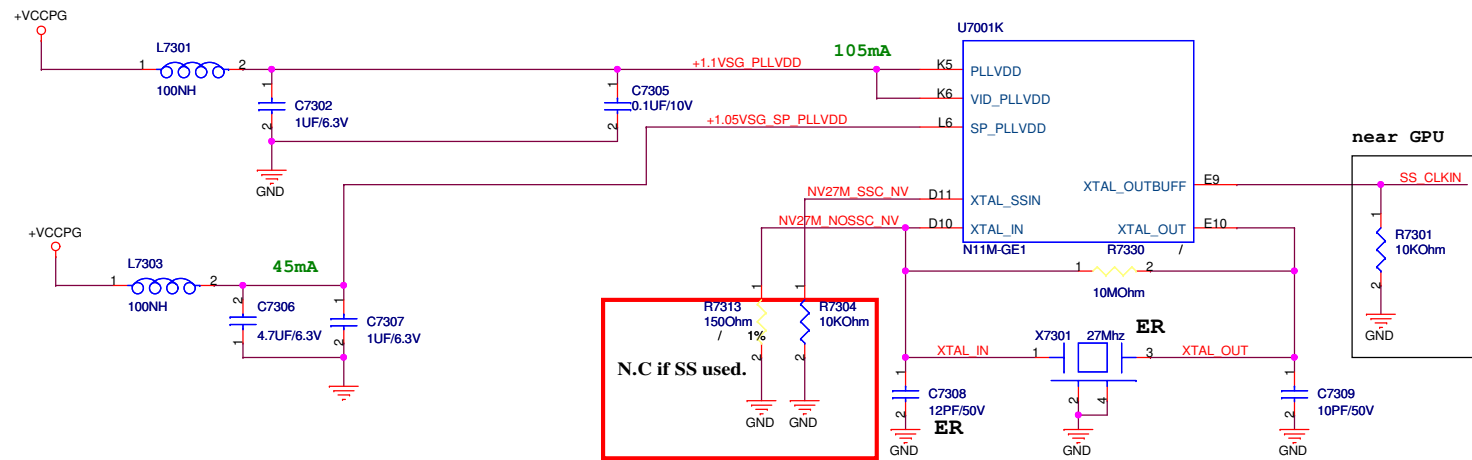
STRAPS	PIN	DESCRIPTION
XCCLK	ROM_SO	Control the output frequency of the internal PCI-Busgen Clock. This must be strapped to logic** for correct functionality. 0 = 270MHz (Default) 1 = Reserved
FB_0_BAR_SIZE	ROM_SO	Select the system frame buffer aperture size used by the GPU. 0 = 32MB (Default) 1 = Reserved
SMBALT_ADDR	ROM_SO	Configure the I/O address of a GPU. 0 = Disabled 1 = GACS (Mail-Box usage)
VGA_DEVICE	ROM_SO	Used to identify the device type of the GPU within the PCI configuration space. As ID DeviceClassCode 302H 1 = VGA Device (Default=Class Code 302H)
PCI_DEVID[4]	ROM_SCLK	nVIDIA GPU PCI Device IDs straps(Refer to PUN or Datasheet)
SUB_VENDOR	ROM_SCLK	Determines if the VBIOS is integrated with SBIOS/ROM not present or if it is in a separate video ROM/ROM present. 0 = No Video BIOS ROM 1 = BIOS ROM is present (Default)
SLOT_CLK_CFG	ROM_SCLK	Pull this strap high if the GPU and MCM share common PCI Express reference clock, for example from the same clock generator chip. As GPU & MCM not share 0 = GPU & MCM share (Default) 1 = Disable PCI Express
PEX_PL1_EN_THERM	ROM_SCLK	To <u>enable</u> the PCI Express PL1 termination enable. 0 = Disable 1 = Enable
PCI_DEVID[3:0]	STRAP2	nVIDIA GPU PCI Device IDs are typically specified in the 32-bit register PCI_W0[31:0]. Bits[31:5] are fixed in silicon(bits[4:3] can be changed using the PCI_DEVID straps). Refer to the relevant data sheets & PUN for the PCI Device ID information.

Physical Strapping Pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_FLL_EN_TH
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP1	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP2	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Value	Pull-Up to VDD	Pull-Down to GND
5K Ω	1000	0000
10K Ω	1001	0001
15K Ω	1010	0010
20K Ω	1011	0011
25K Ω	1100	0100
30K Ω	1101	0101
35K Ω	1110	0110
45K Ω	1111	0111

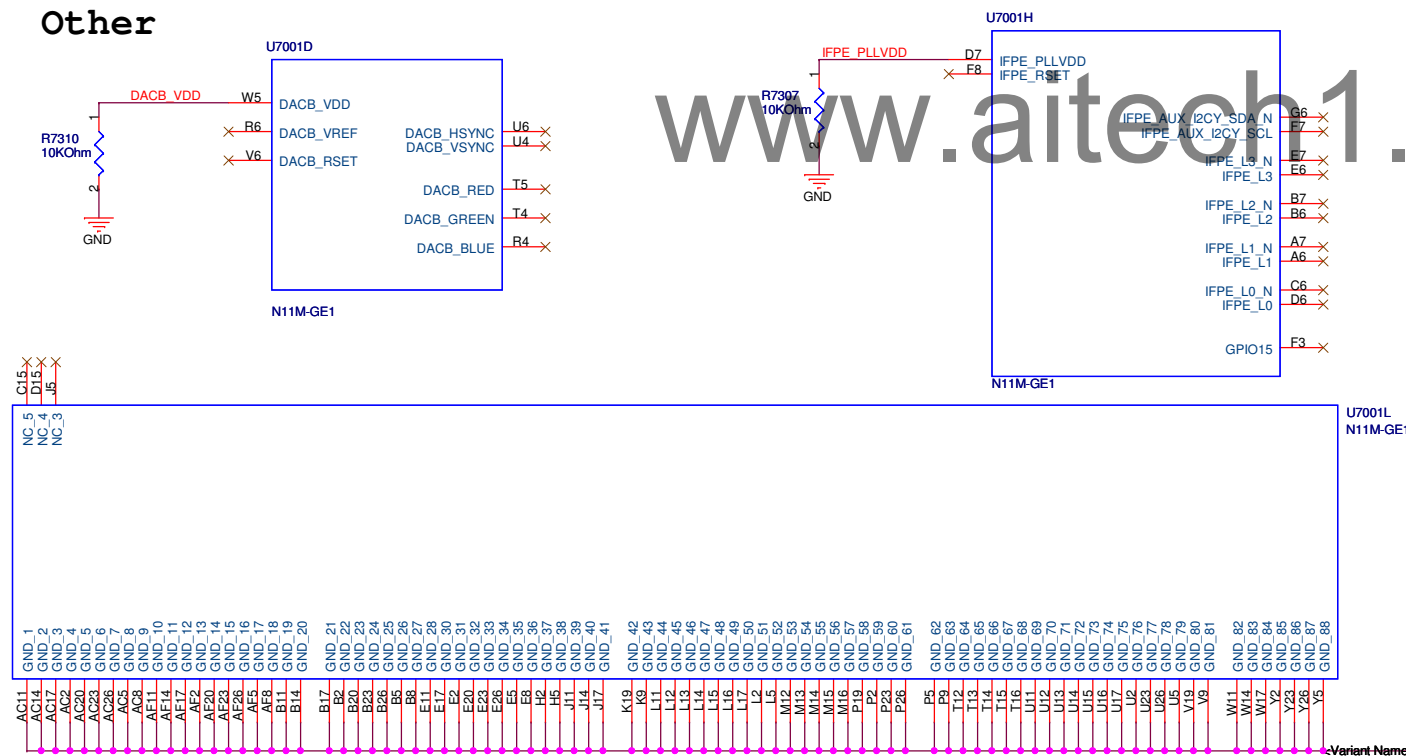
STRAPS	PIN	DESCRIPTION
RAMCFG[3:0]	ROM_SI	MEMORY TYPE, MAKE AND SIZE INFO ▼ 0010 - DDR3 64Kx16 HYNIX/H5TQ10638FR-12C 0011 - DDR3 64Kx16 Samsung/K4W10468-HC12 ... TBD

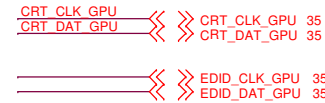
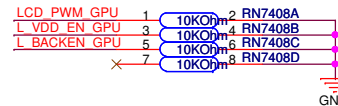
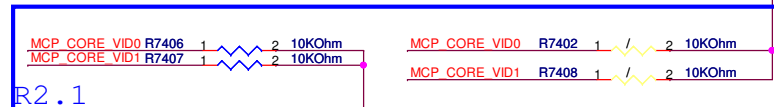
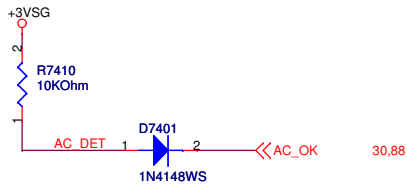
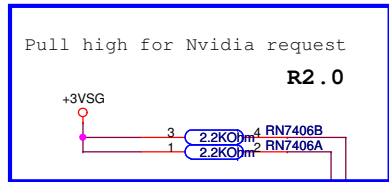
Xtal



ER:加高沒有symbol,先用EPSON的

Other





R2.0



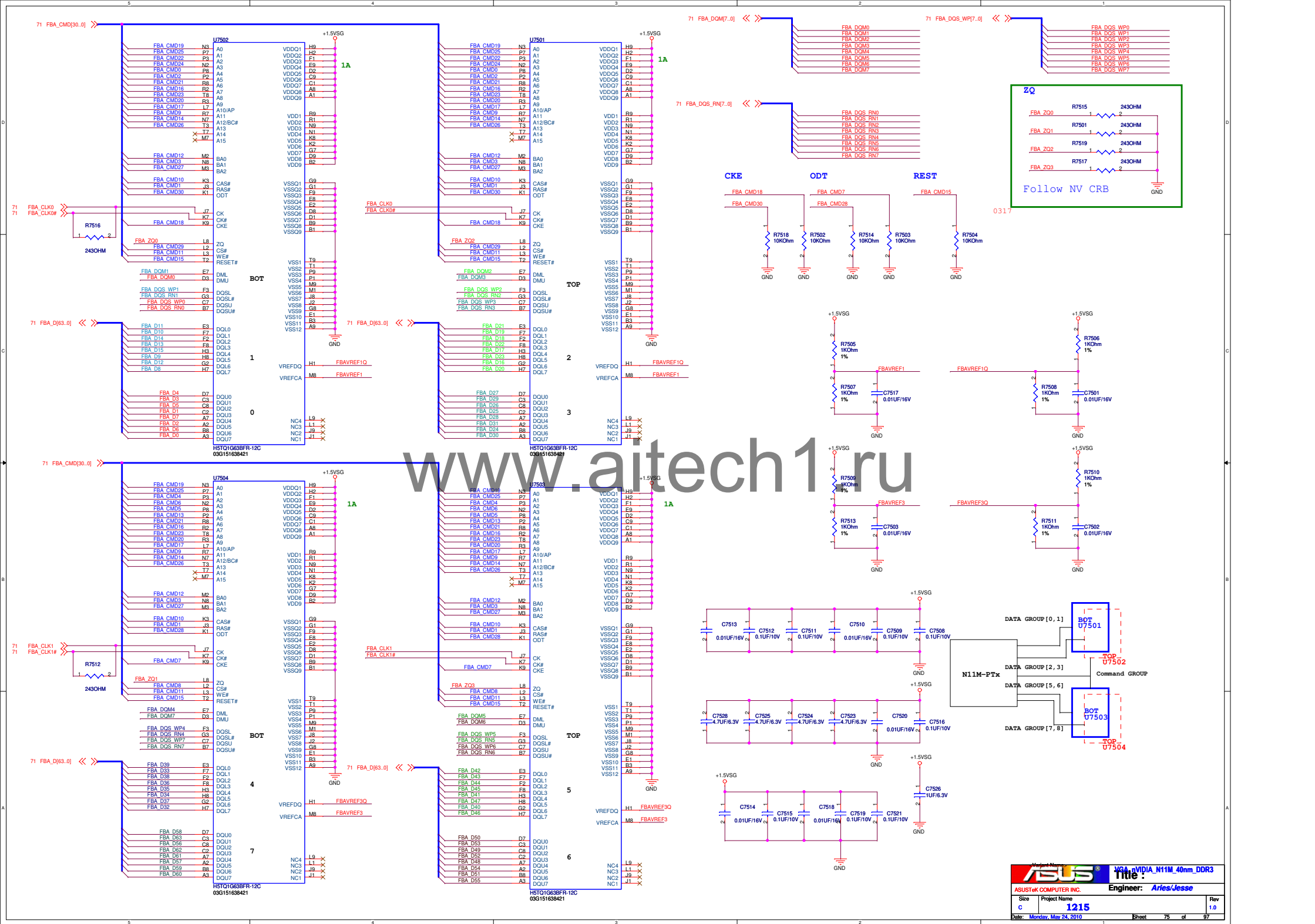
GPIO ASSIGNMENTS

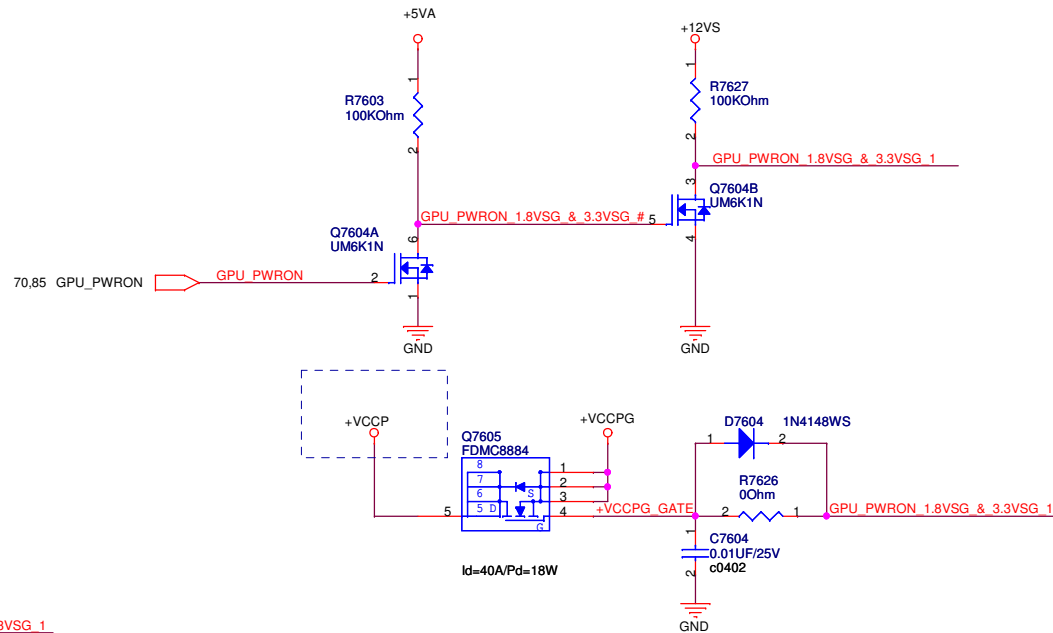
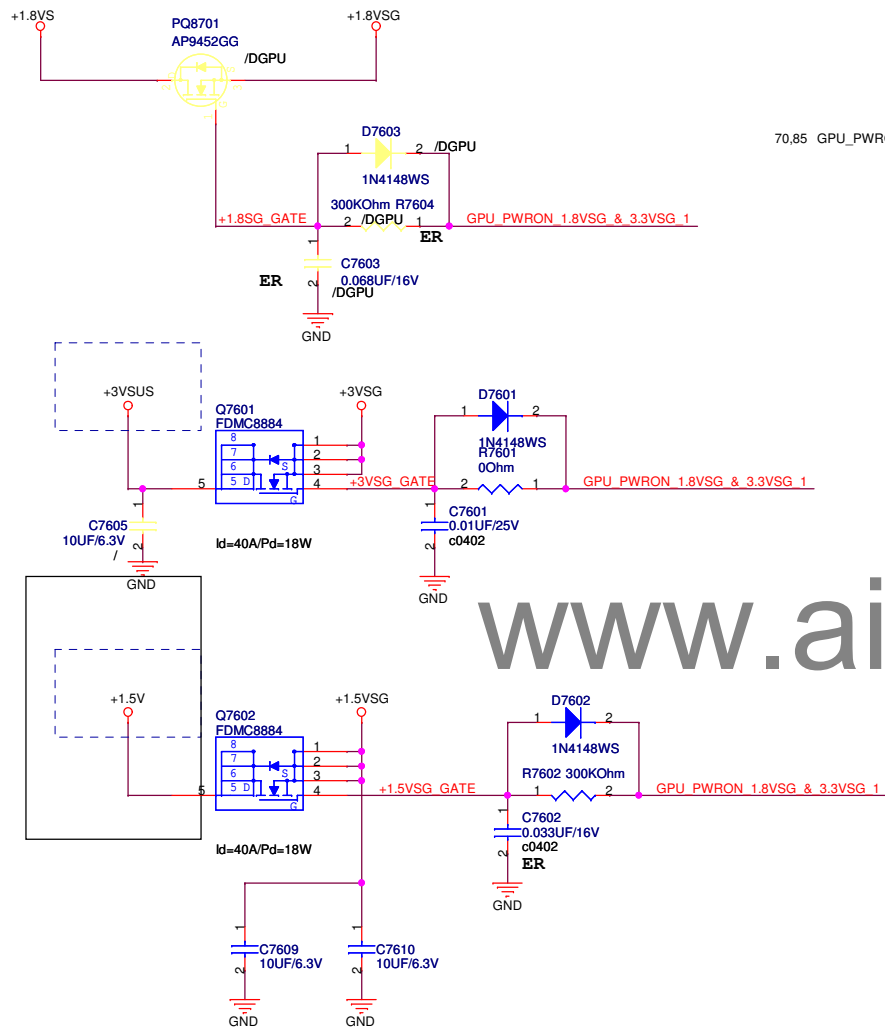
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	NVGEM
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	HIGH	NVVDD VID 0
6	OUT	HIGH	NVVDD VID 1
7	OUT	HIGH	FBVDD VID 0
8	IN/OUT	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	HIGH	FBVREF SELECT
11	OUT	HIGH	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL 0
14	OUT	HIGH	PS CONTROL 1

MCP_CORE_VID0	MCP_CORE_VID1	+0.89VS
L	L	0.848V
H	L	0.896V
H	H	0.945V
L	H	0.896V

<Variant Name>

ASUS		Title : VGA_nVIDIA_N11M-GE2_GPIO	
ASUSTeK COMPUTER INC		Engineer: Aries/Jesse	
Size	Project Name	Rev	
Custom	1215	1.0	
Date: Monday, May 24, 2010		Sheet	74 of 97






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<Variant Name>

ASUS		Title : VGA-Power	
ASUSTeK COMPUTER INC		Engineer: <i>Aries/Jesse</i>	
Size B	Project Name 1215		Rev 2.1
Date: Monday, May 24, 2010		Sheet	76 of 97


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<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size A	Project Name UL20A		Rev 2.1
Date: <u>Monday, May 24, 2010</u>		Sheet	77 of 97


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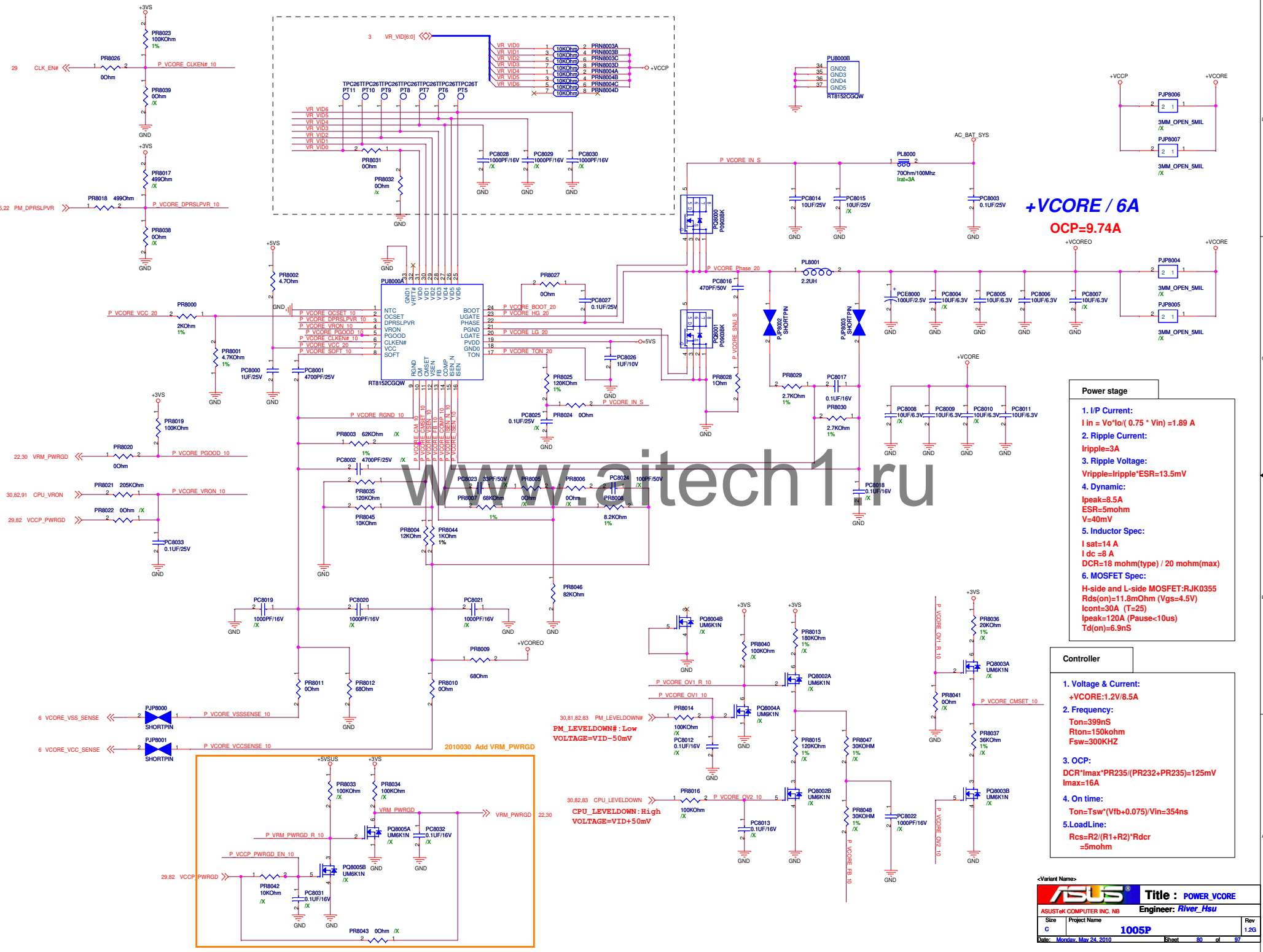
<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size A	Project Name UL20A		Rev 2.1
Date: <u>Monday, May 24, 2010</u>		Sheet	78 of 97

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<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer: <i>Jerry Yu</i>	
Size <i>A</i>	Project Name UL20A		Rev <i>2.1</i>
Date: <i>Monday, May 24, 2010</i>		Sheet	79 of 97

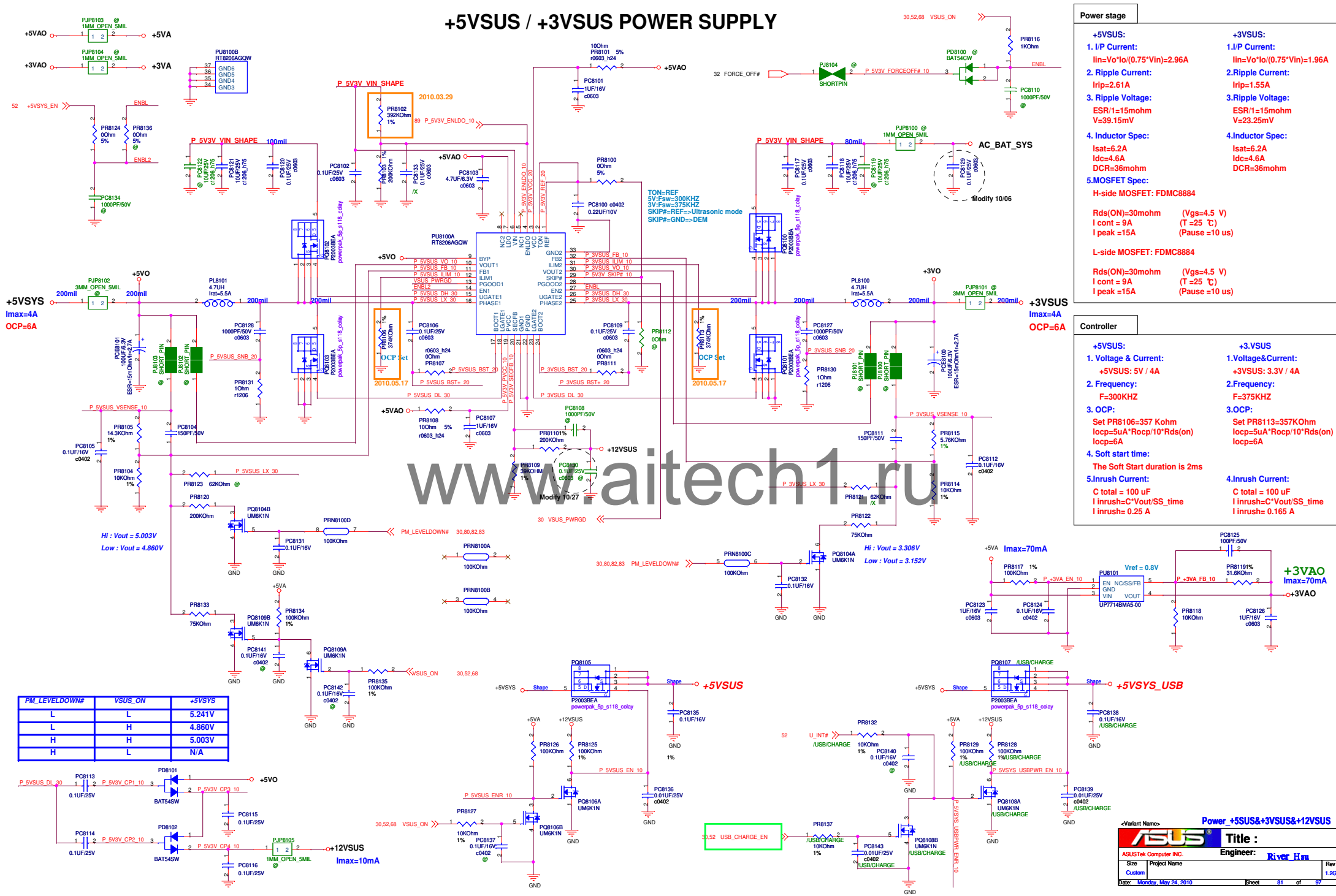


+VCORE / 6A
OCP=9.74A

- Power stage**
 - I/P Current:**
 $I_{in} = V_o/I_o / (0.75 \cdot V_{in}) = 1.89 \text{ A}$
 - Ripple Current:**
Irripple=3A
 - Ripple Voltage:**
Vripple=Irripple*ESR=13.5mV
 - Dynamic:**
Ipeak=8.5A
ESR=5mohm
V=40mV
 - Inductor Spec:**
I sat=14 A
I dc =8 A
DCR=18 mohm(type) / 20 mohm(max)
 - MOSFET Spec:**
H-side and L-side MOSFET:RJK0355
Rds(on)=11.8mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)
Td(on)=6.9nS

- Controller**
 - Voltage & Current:**
+VCORE:1.2V/8.5A
 - Frequency:**
Ton=399nS
Rton=150kohm
Fsw=300KHZ
 - OCP:**
DCR*I_{max}*(PR235/(PR232+PR235))=125mV
I_{max}=16A
 - On time:**
Ton=Tsw*(Vfb+0.075)/Vin=354ns
 - Load Line:**
Rcs=R2/(R1+R2)*Rdcr
=5mohm

+5VSUS / +3VSUS POWER SUPPLY



Power stage

+5VSUS:

- 1. I/P Current:**
 $I_{in} = V_o / I_o / (0.75 \cdot V_{in}) = 2.96A$
- 2. Ripple Current:**
 $I_{rip} = 2.61A$
- 3. Ripple Voltage:**
 $ESR / 1 = 15m\Omega$
 $V = 39.15mV$
- 4. Inductor Spec:**
 $I_{sat} = 6.2A$
 $I_{dc} = 4.6A$
 $DCR = 36m\Omega$
- 5. MOSFET Spec:**
H-side MOSFET: FDMC8884

 $R_{ds(ON)} = 30m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 9A$ ($T = 25^\circ C$)
 $I_{peak} = 15A$ (Pause ≥ 10 us)

L-side MOSFET: FDMC8884

 $R_{ds(ON)} = 30m\Omega$ ($V_{gs} = 4.5V$)
 $I_{cont} = 9A$ ($T = 25^\circ C$)
 $I_{peak} = 15A$ (Pause ≥ 10 us)

+3VSUS:

- 1. I/P Current:**
 $I_{in} = V_o / I_o / (0.75 \cdot V_{in}) = 1.96A$
- 2. Ripple Current:**
 $I_{rip} = 1.55A$
- 3. Ripple Voltage:**
 $ESR / 1 = 15m\Omega$
 $V = 23.25mV$
- 4. Inductor Spec:**
 $I_{sat} = 6.2A$
 $I_{dc} = 4.6A$
 $DCR = 36m\Omega$

Controller

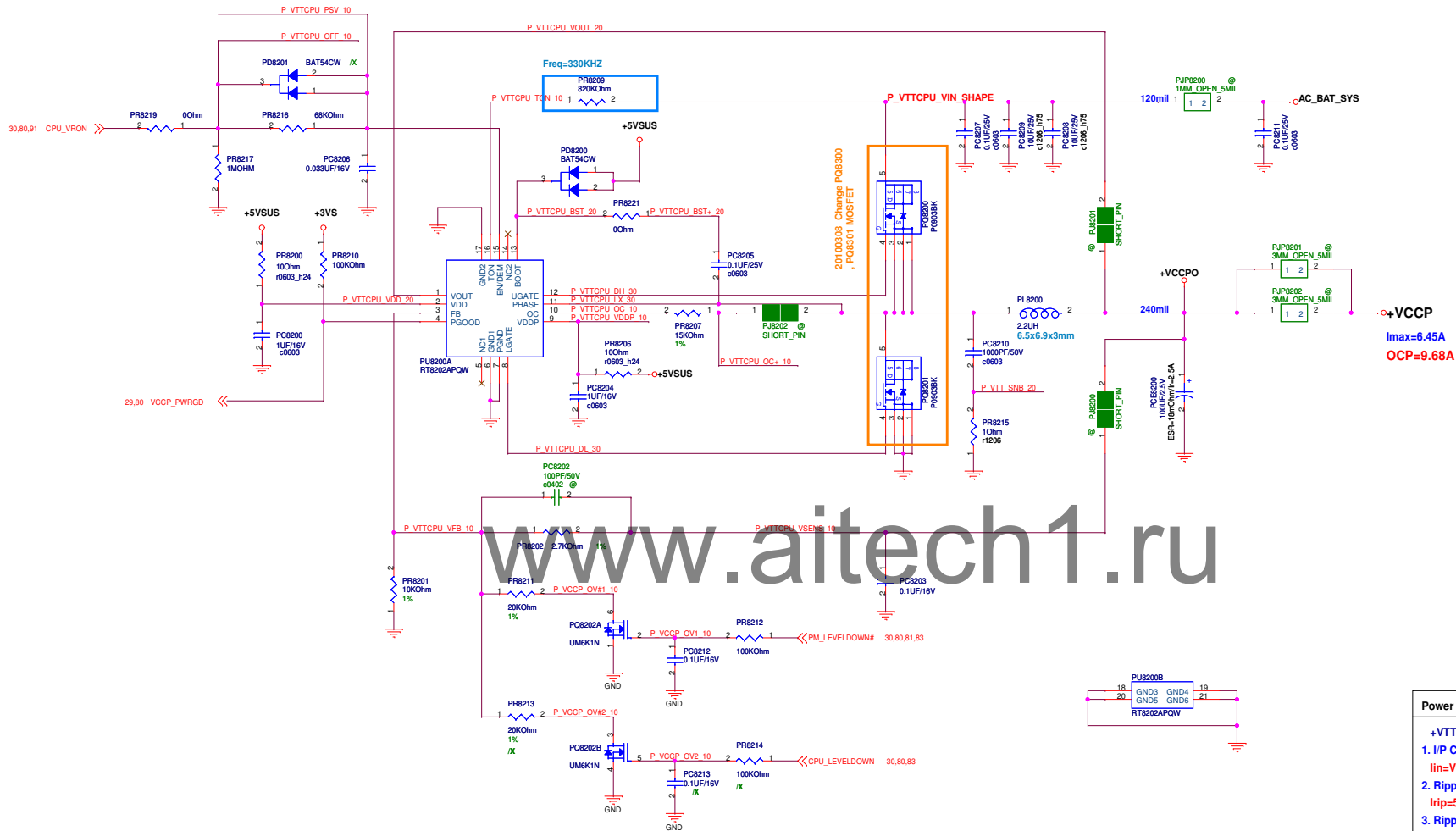
+5VSUS:

- 1. Voltage & Current:**
+5VSUS: 5V / 4A
- 2. Frequency:**
 $F = 300KHZ$
- 3. OCP:**
Set PR8106 = 357 Kohm
 $I_{ocp} = 5uA \cdot R_{ocp} / 10 \cdot R_{ds(on)}$
 $I_{ocp} = 6A$
- 4. Soft start time:**
The Soft Start duration is 2ms
- 5. Inrush Current:**
 $C_{total} = 100 uF$
 $I_{inrush} = C \cdot V_{out} / SS_time$
 $I_{inrush} = 0.25 A$

+3VSUS:

- 1. Voltage & Current:**
+3VSUS: 3.3V / 4A
- 2. Frequency:**
 $F = 375KHZ$
- 3. OCP:**
Set PR8113 = 357 Kohm
 $I_{ocp} = 5uA \cdot R_{ocp} / 10 \cdot R_{ds(on)}$
 $I_{ocp} = 6A$
- 4. Inrush Current:**
 $C_{total} = 100 uF$
 $I_{inrush} = C \cdot V_{out} / SS_time$
 $I_{inrush} = 0.165 A$

+VCCP

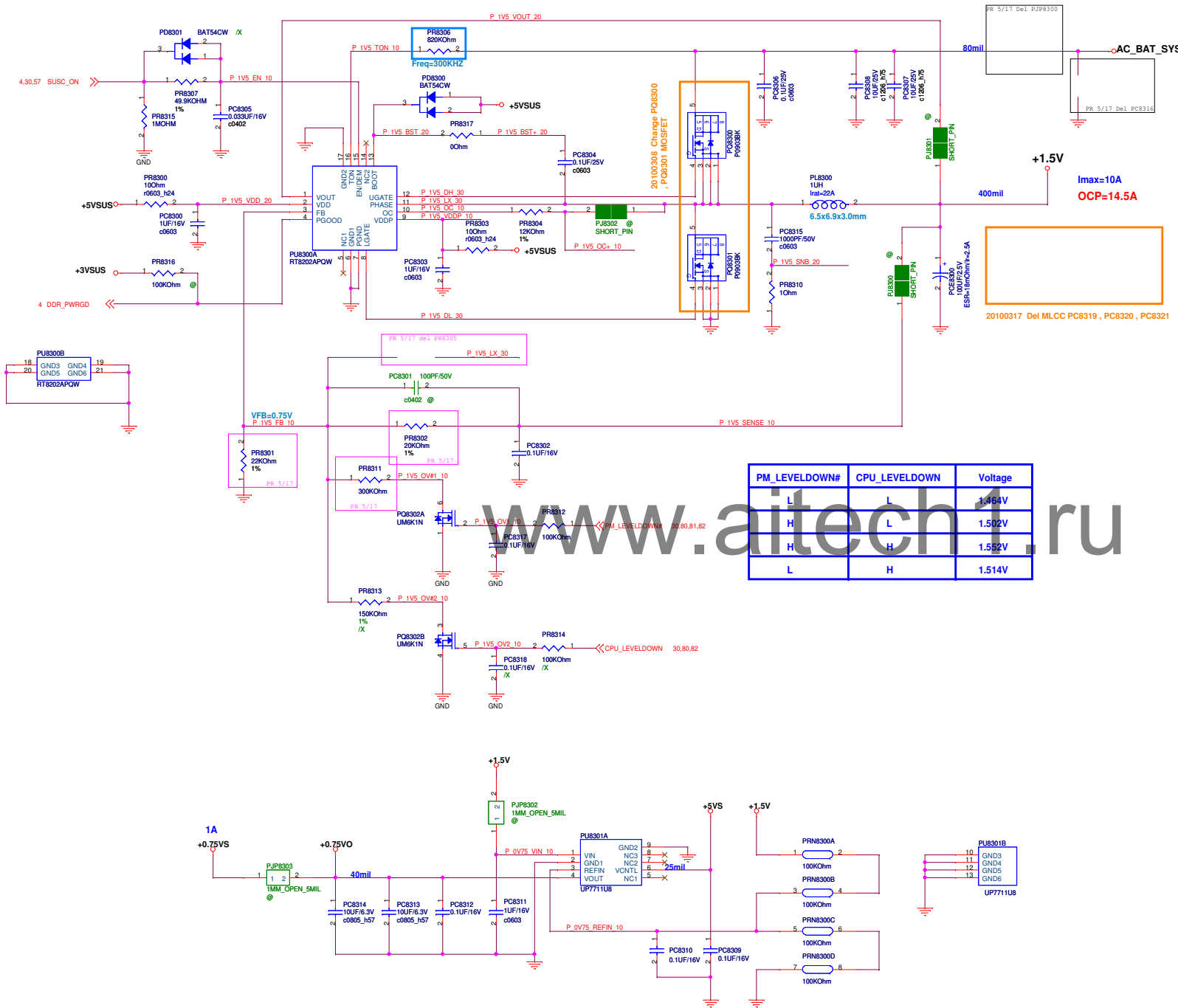


PM_LEVELDOWN#	CPU_LEVELDOWN	CPU_LEVELDOWN#	Voltage	Status
L	L	H	0.953V	Power Saving
H	L	H	1.054V	Normal
H	H	L	N/A	Performance
L	H	L	N/A	N/A

Controller	
+VTT_CPU:	
1. Voltage & Current:	
+VTT_CPU:	1.05V / 15A
2. Frequency:	
F=	330KHZ
3. OCP:	
Set PR8207=	4.99 Kohm
loccp=Rocp	20uA/Rds(on)
loccp=	26A
4. Soft start time:	
The SS duration is	1.35ms
5.Inrush Current:	
C total =	440 uF
I inrush=C*Vout/SS_time	
I inrush=	0.342 A

Power stage	
+VTT_CPU:	
1. I/P Current:	
lin=Vo*Io/(0.75*Vin)=2.33A	
2. Ripple Current:	
Irip=5.36A	
3. Ripple Voltage:	
ESR/2=7.5mohm	
Vripple=40.26mV	
4. Inductor Spec:	
Isat=40A	
Idc=25A	
DCR=1.6mohm	
5.MOSFET Spec:	
H-side MOSFET: RJK0355DPA	
Rds(ON)=16.5mohm (Vgs=4.5 V)	
I cont = 30A	(T =25 °C)
I peak =120 A	(Pause =10 us)
L-side MOSFET: RJK0353DPA	
Rds(ON)=7.6mohm (Vgs=4.5 V)	
I cont = 35A	(T =25 °C)
I peak =140 A	(Pause =10 us)

+1.8V & +0.9VS POWER SUPPLY



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage
L	L	1.454V
H	L	1.502V
H	H	1.552V
L	H	1.514V

Power stage

DDR III:

- I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.22A$
- Ripple Current:**
 $I_{rip} = 4.62A$
- Ripple Voltage:**
 $ESR / 1 = 15mohm$
 $V = 69.3mV$
- Inductor Spec:**
 $I_{sat} = 12.7A$
 $I_{dc} = 9.5A$
 $DCR = 8.5mohm$
- MOSFET Spec:**
H-side MOSFET: RJK0355DPA
 $R_{ds(ON)} = 16.5mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^{\circ}C$)
 $I_{peak} = 120A$ (Pause = 10 us)
- L-side MOSFET: RJK0355DPA**
 $R_{ds(ON)} = 16.5mohm$ ($V_{gs} = 4.5V$)
 $I_{cont} = 30A$ ($T = 25^{\circ}C$)
 $I_{peak} = 120A$ (Pause = 10 us)


Controller

DDR III:

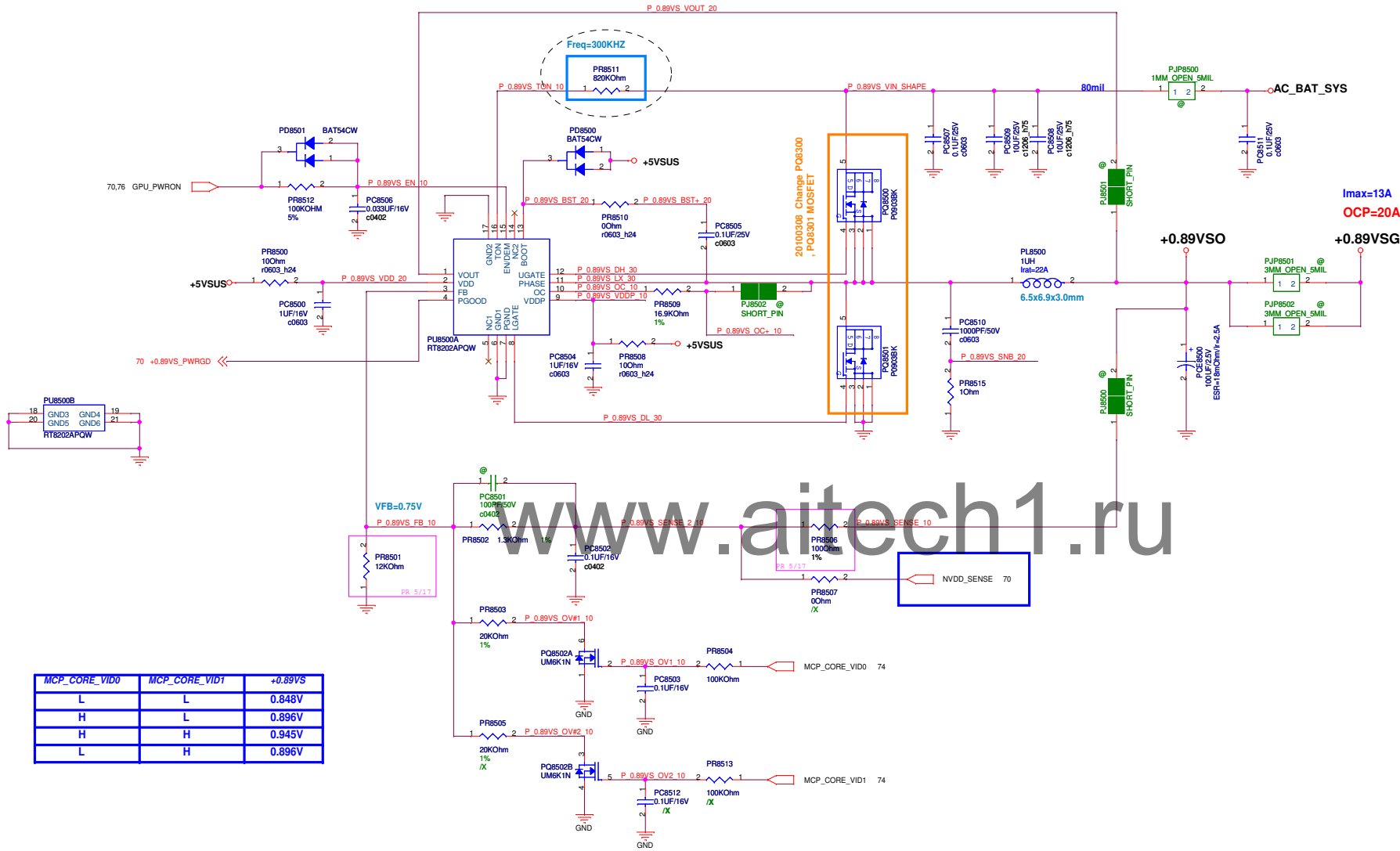
- Voltage & Current:**
 $+1.5V: 1.5V / 10A$
- Frequency:**
 $F = 300KHZ$
- OCP:**
Set $R_{8302} = 12Kohm$
 $I_{ocp} = R_{ocp} \cdot 20uA / R_{ds(on)}$
 $I_{ocp} = 14.3A$
- Soft start time:**
The Soft Start duration is 1.35ms
- Inrush Current:**
 $C_{total} = 220uF$
 $I_{inrush} = C \cdot V_{out} / SS_time$
 $I_{inrush} = 0.244A$

1. Voltage & Current:
 $+0.75V: 0.75V / 1A$

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<Variant Name>			
		Title : +1.8V & VTDDR	
ASUSTek Computer INC.		Engineer: River_Hsu	
Size	Project Name		Rev
C	1005P		1.2G
Date: Monday, May 24, 2010		Sheet	84 of 97

GPU NVDD POWER SUPPLY



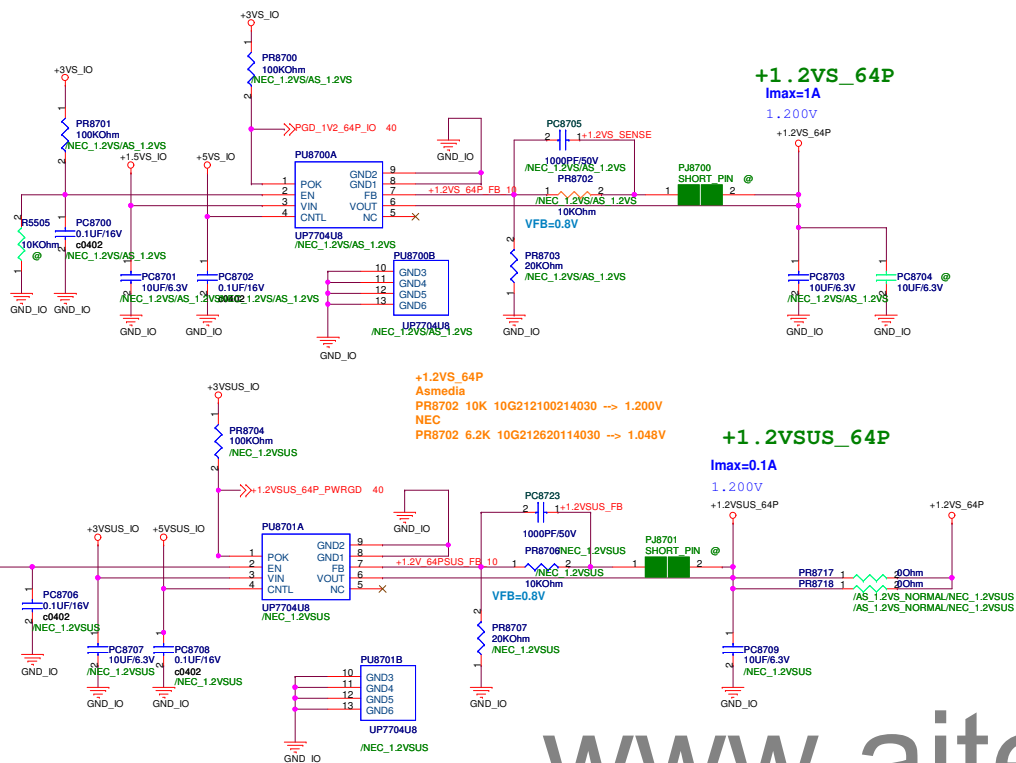
Power stage	
NVDD:	
1. I/P Current:	$I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 2.11A$
2. Ripple Current:	$I_{rip} = 7.59A$
3. Ripple Voltage:	$ESR/2 = 7.5m\Omega$ $V = 56.925mV$
4. Inductor Spec:	$I_{sat} = 26A$ $I_{dc} = 17.5A$ $DCR = 4.2m\Omega$
5. MOSFET Spec:	H-side MOSFET: RJK0355DPA L-side MOSFET: RJK0353DPA
	$R_{ds(ON)} = 16.5m\Omega$ ($V_{gs} = 4.5V$) $I_{cont} = 30A$ ($T = 25^\circ C$) $I_{peak} = 120A$ (Pause = 10 us)
	$R_{ds(ON)} = 7.6m\Omega$ ($V_{gs} = 4.5V$) $I_{cont} = 35A$ ($T = 25^\circ C$) $I_{peak} = 140A$ (Pause = 10 us)

Controller	
NVDD:	
1. Voltage & Current:	+NVDD: 0.95V / 15A
2. Frequency:	F = 253KHZ
3. OCP:	Set R8504 = 7.5 Kohm $I_{ocp} = R_{ocp} \cdot 20uA / R_{ds(on)}$ $I_{ocp} = 20A$
4. Soft start time:	The Soft Start duration is 1.35ms
5. Inrush Current:	C total = 440 uF $I_{inrush} = C \cdot V_{out} / SS_time$ $I_{inrush} = 0.310A$

<Variant Name>

ASUS		Title : POWER_I/O_NVDD	
ASUSTek COMPUTER INC. NBI		Engineer: Matt_Wang	
Size	Project Name		Rev
Custom		Design IP	1.0
Date: Monday, May 24, 2010	Sheet	85	of 97

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Dual layout BOM table	OPTIONAL CHOICE	Voltage (NEC=1.05V;ASM=1.2V)
NEC (Normal)	/NEC_1.2VS/AS_1.2VS	NEC PR8702 6.2K 10G212620114030 --> 1.048V
NEC (SUS)	/NEC_1.2VSUS	NEC PR8706 6.2K 10G212620114030 --> 1.048V
ASM1042 (Normal)	/NEC_1.2VS/AS_1.2VS /AS_1.2VS_ALL NORMAL	Asmedia PR8702 10K 10G212100214030 --> 1.200V
ASM1042 (Normal +SUS)	/NEC_1.2VS/AS_1.2VS /NEC_1.2VSUS	Asmedia PR8702 10K 10G212100214030 --> 1.200V Asmedia PR8706 10K 10G212100214030 --> 1.200V

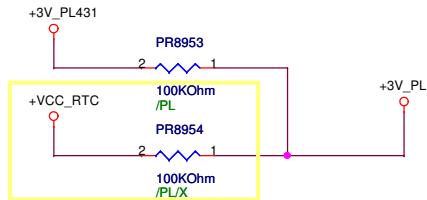
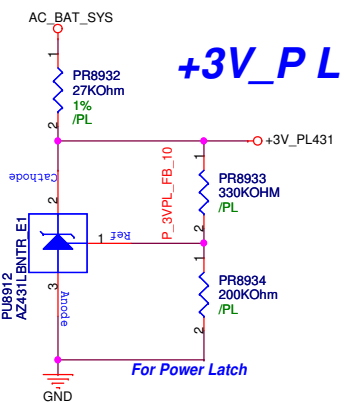
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Dual layout BOM table	BOM(USB interface)	BOM(PCIe interface)	BOM(XTL interface)	BOM(SPI interface)
ASM only (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B	R4038, R4039, R4040, R4041, C4042, C4043	X4002(20MHZ, 07G010012000), @C4036, C4037(22pF, 11G232022004030), C4051, R4032, @C4052	R4053, R4054, R4055, R4056, R4028/ R4029 (4.7K, 10G212472004030), C4003, U4007
NEC only (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B	R1318, R1319, R1320, R1321, C1325, C1326	X4002(24MHZ, 11G232027004070), C4036, C4037(12pF, 11G232012004320), @C4051, R1317, @R1315, @R1316	R1324, R1325, R1326, R1327, R4028(8.2K, 10G212822004030), R4029(39.2K, 10G212392214031), C4003, U4007
PCH only (USB2.0)	RN4013A, RN4013B			
ASM+PCH (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B, RN4013A, RN4013B	R4038, R4039, R4040, R4041, C4042, C4043		
NEC+PCH (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B, RN4013A, RN4013B	R1318, R1319, R1320, R1321, C1325, C1326		

<Variant Name>

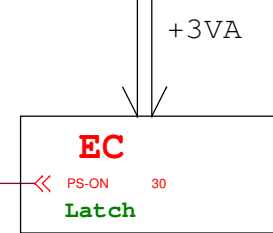
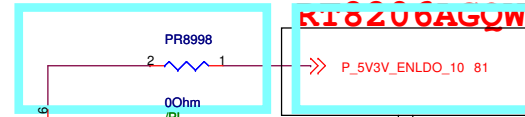
ASUS		Title : N/A	
ASUSTek COMPUTER INC. NB		Engineer: Aaron_Lin	
Size Custom	Project Name	UL20A	Rev 1.0
Date: Monday, May 24, 2010		Sheet 87 of 87	





Power Latch table :

BAT	A/D_DOCK_IN		Mode
1	X	BAT /X	Latch
0	1	ADP, BAT	Out
0	0	ADP /X	Latch

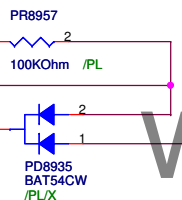
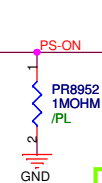
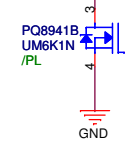
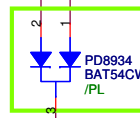
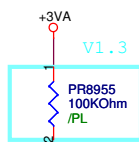


30 PWR_SW_EC#

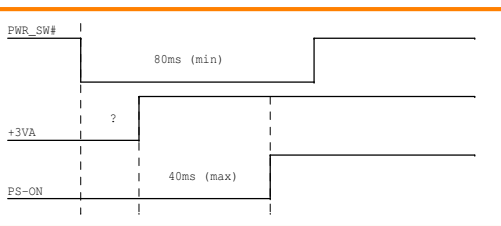
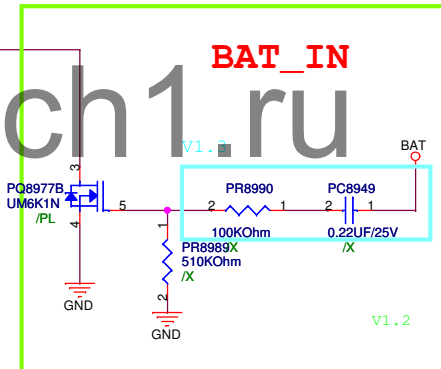
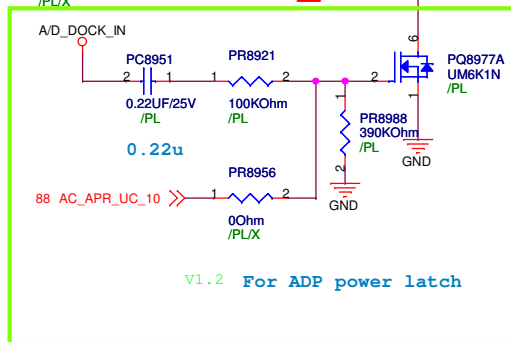
68 PWR_SW#

30 EPX_GATE_EC#

69 EPX_GATE_SW#

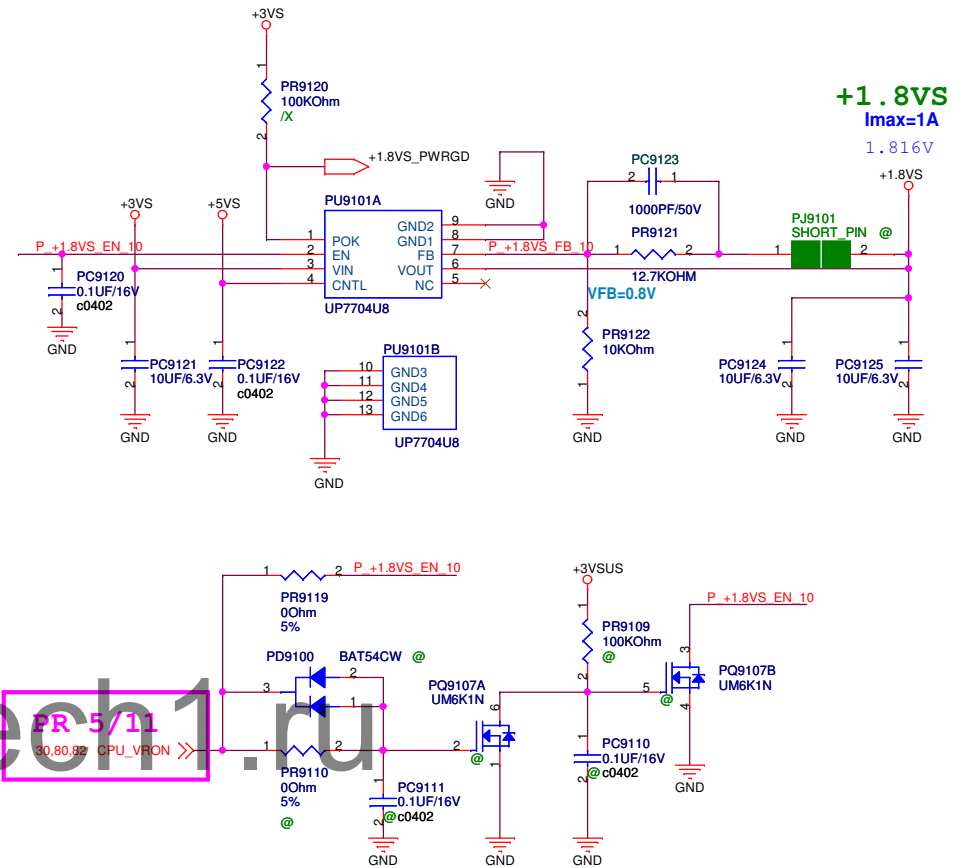
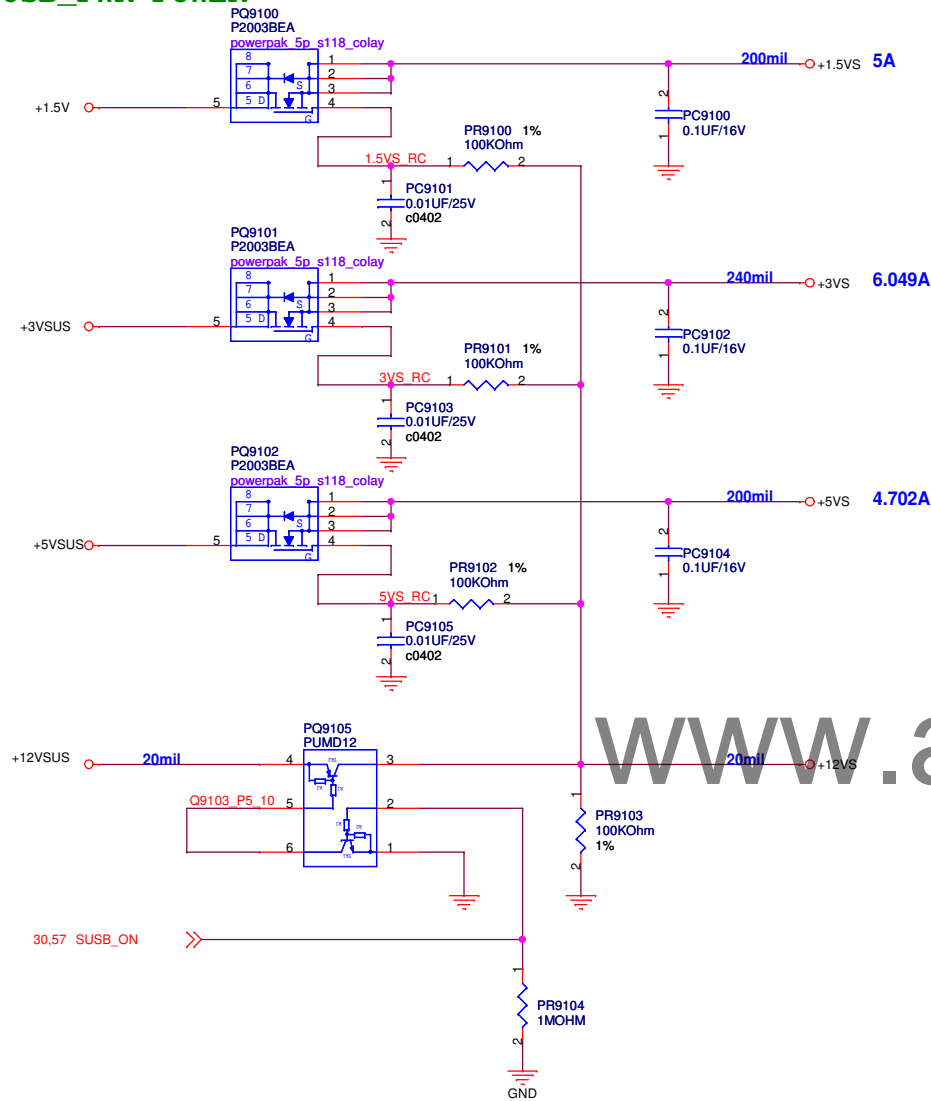


ADP_IN



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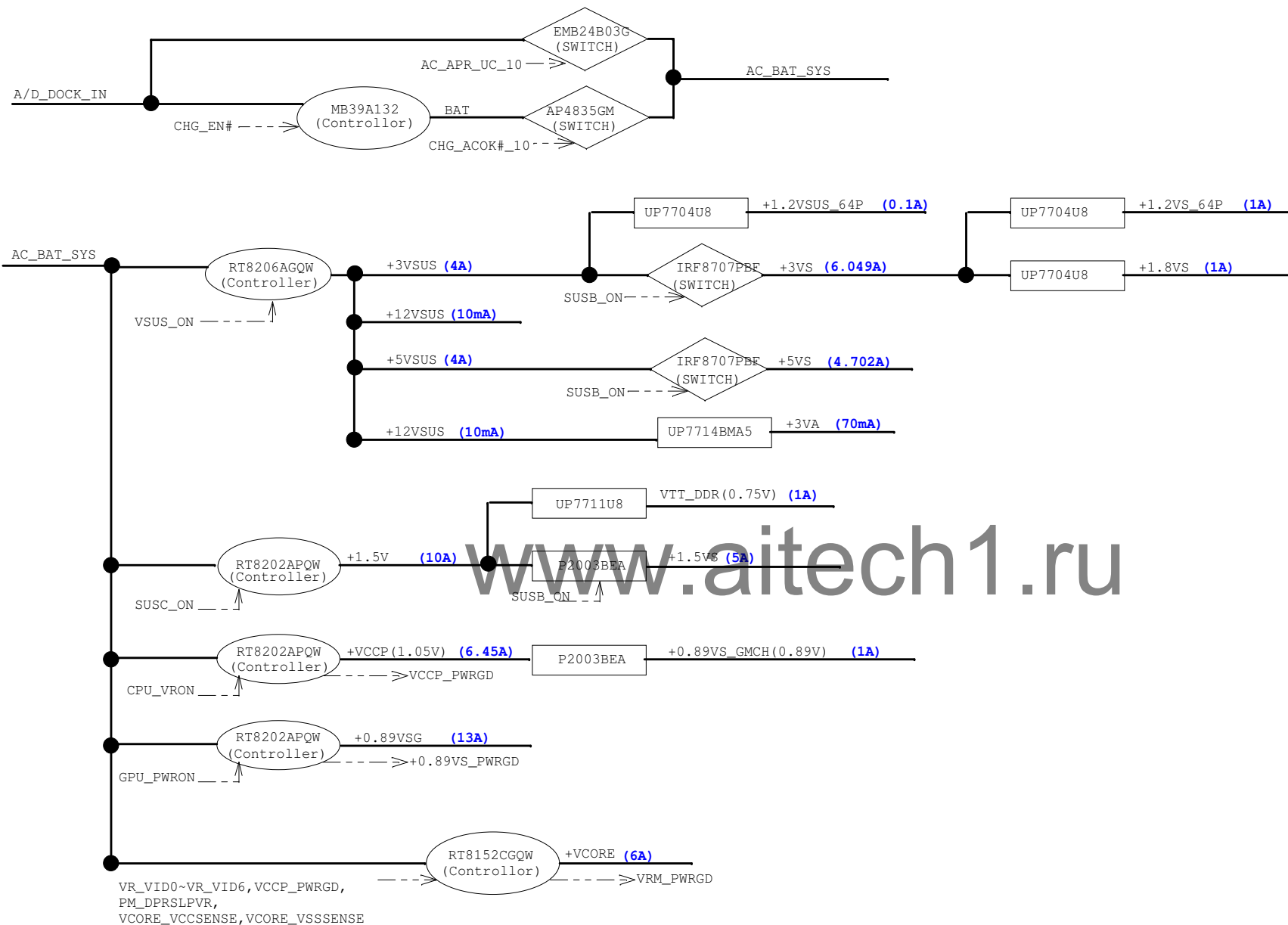
SUSB_PWR POWER



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<Variant Name>

ASUS		Title: POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Matt_Wang	
Size B	Project Name Design_IP	Rev 1.0	
Date: Monday, May 24, 2010		Sheet 91 of 97	



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PEGATRON		Title : POWER_HISTORY	
BU2-Power Div-Power Dept.2		Engineer: Ian Chung	
Size C	Project Name UL80VT	Rev 3.12	
Date: Monday, May 24, 2010		Sheet	93 of 97

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3/29 Update to DDR3_Shangyu
3/29 Add J5501 POWER Button/LED Conn._Shangyu
3/29 Add J6901 Express Gate Button Conn._Shangyu
3/30 Add J5602 T/P Conn._Shangyu
3/30 Switch Express Gate & Wifi Button._Shangyu
3/31 Change CPU DDR3 Voltage_Shangyu
3/31 Change Discharge DDR3 Voltage_Shangyu
3/31 Add TP 00hm_Shangyu
4/6 Add DC Jack
5/11 P.04 DDR3_PWROK chang to DDR_PWRGD_Kaiyu
5/11 P.91 P_+1.8VS_EN_10 control change to CPU_VRON_Kaiyu
5/12 P.46 add +3VS_LCD discharge_Kaiyu
5/12 P.67 BToB Pin 15,16 change to Pin 42,43_Kaiyu
5/12 P.68 BToB Pin 15,16 change to Pin 42,43_Kaiyu
5/12 P.46 C4626 change to 0.1uF_Kaiyu
5/12 P.60 EMI ESD check Pass D6005 change optional to @_Kaiyu
5/12 P.37 EMI ESD +/-2K Pass D3702/D3703 change optional to @_Kaiyu
5/12 P.81 EMI ESD +/-2K Pass D3702/D3703 change optional to @_Kaiyu
5/13 P.29 C_LAN_25M_R add 8.2K ohm pull Hi_Kaiyu
5/14 P.47 D4702 change optional to @_Kaiyu
5/17 P.29 C_LAN_25M add 33p for EMI_Kaiyu
5/17 P.29 R2932change to 47ohm for EMI_Kaiyu
5/17 P.22 RN2209 change to 47ohm*4 for EMI_Kaiyu
5/17 P.22 C2201 22pF change to 10pF for EMI_Kaiyu
5/17 P.38 MIC_CLK_R add 33P to GND for EMI_Kaiyu
5/17 P.38 MIC_DATA_R add 33P to GND for EMI_Kaiyu
5/17 P.69 J6901 pin3 change conn. to GND_Kaiyu
5/17 Power Modify BOM
P81 : PR8106 change to 374K 0402 1%
PR8113 change to 374K 0402 1%
P83 : Del PR8305 PJP8300 PC8316
PR8301 change to 22K 0402 1%
PR8302 change to 20K 0402 1%
PR8311 change to 300K 0402 1%
PR8316 change to @
P85 : PR8501 change to 12K 0402 1%
PR8506 change to 100-OHM 0402 1%
5/17 P.61 all part optional change to @_Kaiyu
5/18 P.67 BToB Pin 15,16 & 42,43 Swap(change back)_Kaiyu
5/18 P.68 BToB Pin 15,16 & 42,43 Swap(change back)_Kaiyu
5/18 P.52 add R5254 pullhi to +3Vsus for BIOS detect_Kaiyu
5/18 P.50 SWAP RN5001A & add RN5001B for Layout Request_Kaiyu
IO 5/19 P.40 U6903,U6903 Change to 06G030099010 for NB design ip_Kaiyu
IO 5/19 P.33 L3302 Change to 09G028473401 for cost down_Kaiyu
IO 5/19 P.33 U3_PPON1,U3_PPON2 pull 100K to VSUS_3V3_Kaiyu
5/19 P.70 L7001 change PN to 09G013120103_Kaiyu
5/19 P.91 PC9120 optional change to @_Kaiyu

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For Adapter Mode: (1) -> (2) -> (3) -> (4) -> (5) -> ...
 For Battery Mode: (1) -> (2) -> (3) -> (4) -> (4a) -> (4b) -> (5) -> ...

